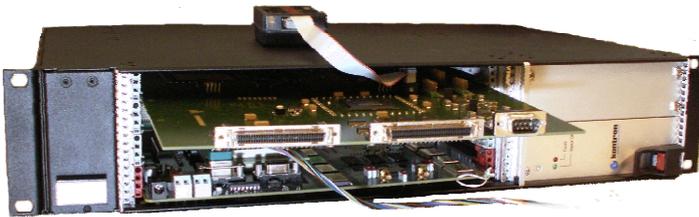




## Executive summary

# On-board Payload Data Processing, for SAR and Multispectral data processing, on-board satellites (LEON2/FFTC)



### Problem area

The On-board Payload Data Processing board (OPDP board) is the flexible solution for SAR and Multispectral data processing, on-board satellites, using a LEON2-FT and the FFTC co-processor.

Satellites in general, and specifically their instruments, are becoming more and more complex every year. There is a continuously demand for more bandwidth, higher sensor resolutions and sensitivities, better data compression, more accurate and adaptive calibration techniques, spacecraft autonomy and many more.

Especially SAR satellites, but also altimeter missions and spectrometry instruments and even SWIR satellites, could highly benefit from fast FFT-oriented processing capabilities. The PowerFFT™ and the FFTC can be controlled from an FPGA, but a much more flexible

solution is in this project created by combining the power of the PowerFFT™ / FFTC with the flexibility of the LEON2 processor.

### Description of work

The consortium consists of

- NLR (prime, h/w, VHDL, s/w)
- Eonic (PowerFFT™ expertise)
- Neways (production)
- Task24 (SDE)
- HybridDSP (SDE)
- 4DSP (VHDL)

The consortium currently develops a demonstration model that shows the principle of operation between the LEON processor and the FFTC. It includes a Software Development Environment for performance analysis.

### Applicability

All satellites that require fast FFT processing could benefit from this development.

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**On-board Payload Data Processing, for SAR and Multispectral data processing, on-board satellites (LEON2/FFTC)**

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## On-board Payload Data Processing, for SAR and Multispectral data processing, on-board satellites (LEON2/FFTC)

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## Abbreviations

AHB	Advance High performance Bus
APB	Advanced Peripheral Bus
BSP	Board Support Package
EM	Engineering Model
EQM	Engineering Qualification Model
FFT	Fast Fourier Transform
FFTC	Fast Fourier Transform Co-processor
FIFO	First-In First-Out
FM	Flight Model
FPGA	Field Programmable Gate Array
I/O	Input / Output
Mcps	Mega complex samples per second
NLR	Nationaal Lucht- en Ruimtevaartlaboratorium (National Aerospace Laboratory)
NSO	Netherlands Space Office
OPDP	On-board Payload Data Processing
PCI	Peripheral Component Interconnect
RTEMS	Real-Time Executive for Multiprocessor Systems
SAR	Synthetic Aperture Radar
SDE	Software Development Environment
SDRAM	Static Dynamic RAM
SF	Switch Fabric
SpW	Space Wire (interface)
SRAM	Static Random Access Memory
SWIR	Short Wave Infrared
TBD	To Be Defined
VHDL	VHSIC Hardware Definition Language (VHSIC is Very High Speed Integrated Circuit)
VME	Versa Module Europe
h/w	Hardware
s/w	Software



## **On-board Payload Data Processing, for SAR and Multispectral data processing, on-board satellites (LEON2/FFTC)**

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### **1. INTRODUCTION**

The On-board Payload Data Processing board (OPDP board) is the flexible solution for SAR and Multispectral data processing, on-board satellites, using a LEON2-FT and the FFTC co-processor.

Satellites in general, and specifically their instruments, are becoming more and more complex every year. There is a continuously demand for more bandwidth, higher sensor resolutions and sensitivities, better data compression, more accurate and adaptive calibration techniques, spacecraft autonomy and many more. Also, one can state that the increasing complexity of spacecraft instruments result in a larger amount of download data, while the available download link capacity increases only slowly.

The tendency in satellites is to perform more data processing on-board, instead of ground processing. First order filtering, adjustments or modifications are to be performed in the on-board electronics in future missions. One special and most difficult mathematical operation is the Fast Fourier Transform. Current space qualified processors aren't fast enough to perform such FFT-processing on the high speed data streams from the current developed instruments. FFT-cores, implemented on FPGAs, are not flexible or fast or enough. In general one can even state that satellite system engineers try avoid complex FFT-operations, as there isn't enough calculation power available in the space market.

All this might change, with the availability of the FFTC: the space qualified version of the PowerFFT™ which is the fastest and most powerful FFT-chip in the world [1][2].

Especially SAR satellites, but also altimeter missions and spectrometry instruments and even SWIR satellites, could highly benefit from fast FFT-oriented processing capabilities. The PowerFFT™ and the FFTC can be controlled from an FPGA, but a much more flexible solution is in this project created by combining the power of the PowerFFT™ / FFTC with the flexibility of the LEON2 processor. [3][4].

This paper presents the capabilities of the “full package solution” of the On-board Payload Data Processing (OPDP) board. This board is currently developed by a Dutch consortium. It not only consists of a hardware solution for high speed FFT-operations, but also provides in the need of a Board Support Package (BSP) and a Software Development Environment: a set of integrated tools for development and testing of mission specific software

Features of the OPDP board are:

- Up to 95 Mcps FFT processing speed (Mcps = Mega complex samples per second)
- Single FFT-operations (up to 1024 points 1D FFT, 1k x 1k points 2D FFT, convolutions, correlations, corrections, etc)
- Multi stage FFT-operations (up to 1 million points 1D FFTs, more complex 2D FFT operations, etc)
- Corner turning of data
- Calculations on data by a LEON2-FT processor
- Sustained data throughput, as there are two memory banks of 128 MByte for storing incoming and outgoing data
- UserBlock for non-standard high-speed data operations (in VHDL, in the control FPGA)

Features of the SDE are:

- Develop, debug, compile and simulate the LEON application
- Define and check the FFTC command sequences
- Determine the FFT performance with the performance profiler
- Toolsuite for building LEON application including a run time library with RTEMS compatible drivers

The consortium consist of: NLR (prime, hardware, VHDL and software), Eonic (architecture, PowerFFT™ expertise), Neways (production), Task24 (Software Development Environment), HybridDSP (SDE) and 4DSP (VHDL).

**2. DEVELOPMENT TRAJECTORY**

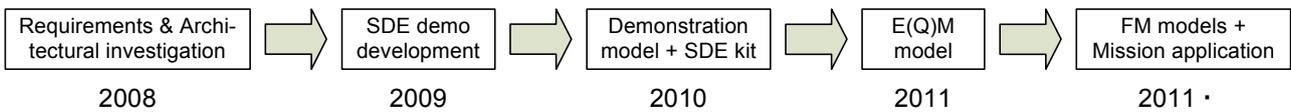


Fig. 1. Timeline of the OPDP development

The timeline of the development of the OPDP is depicted in figure 1. In 2008 a requirements investigation and architectural study has been performed. This resulted in the best trade-off between complexity, flexibility and performance. In 2009 the first set-up of the SDE has been developed, resulting in first issue of the SDE. Now, in 2010, a demonstration model is build that shows the principle of operation between the LEON processor and the FFTC.

**3. FUNCTIONAL BLOCK DIAGRAM**

For the demonstration model a LEON2-FT evaluation board is combined with an in-house designed co-processor board. See figure 2.

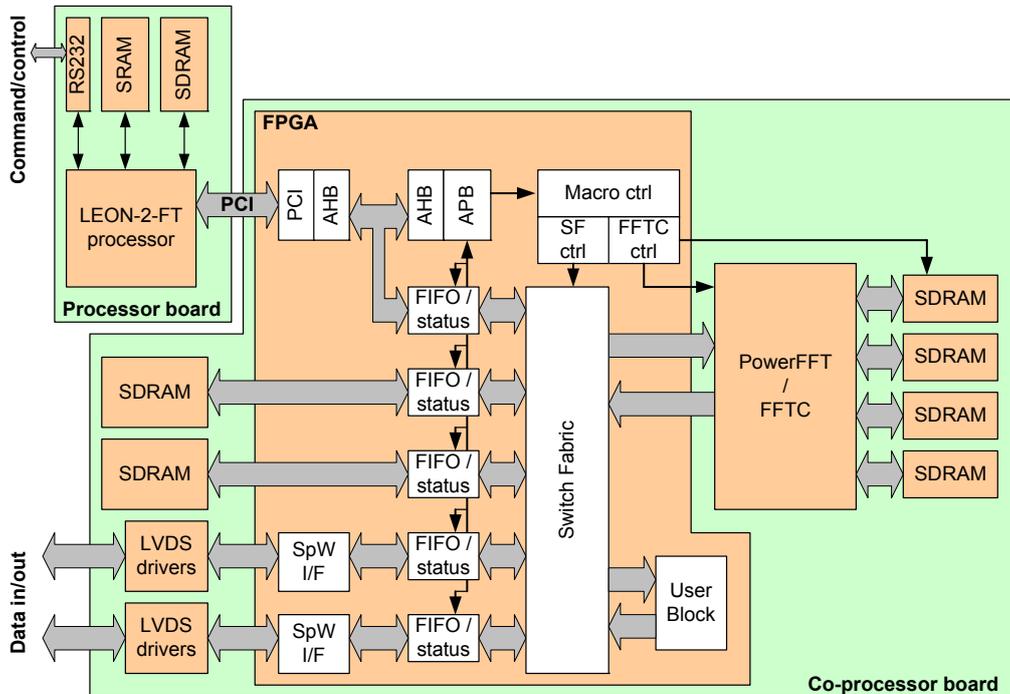


Fig. 2. OPDP block diagram with the LEON2-FT processor board (left) and the designed Co-processor board (right)



For the demonstration board, we purchased the Atmel LEON2-FT processor board. It contains a RS232 port for command/control and it has SDRAM and SRAM for storage of the application and the data. The co-processor board is developed in this project. It currently contains the commercial PowerFFT™ processor, a commercial ProAsic3000 FPGA (for the control) and six commercial SDRAM memory banks. The two boards are connected via a 33 MHz PCI interface.

The PowerFFT™ has four memory ports, connected to 64 MByte memory banks, to store intermediate results or to combine the incoming data with twiddle factors or filtering factors. The FFT-chip and the data-addresses for the memory are all controlled by the FPGA. The input and the output port of the PowerFFT™, the two memory banks, and the I/O interfaces are all connected to a data router called switch fabric in which all data interconnections can be made.

Inside the controller FPGA, there is a PCI to AHB bus block and an AHB to APB bus block. Data and commands can be send from the LEON to the controller FPGA and vice versa. The two SDRAMs (on the left of figure 2) can be used for storage of output results of the PowerFFT™ / FFTC or used for extended FIFO for the input data stream (to enable continuously processing of an input stream of data). Currently SpaceWire interfaces are foreseen, but the board will be extended in the future with High Speed Interfaces, such as SpaceFibre/Wizardlink or GLink interfaces. The central part of the FPGA is the Switch Fabric. Here different data routes can be set. An intelligent SF-controller keeps track of the status of the different routes and will enable a route as soon as it becomes available. The FFTC control block controls all possible commands to the PowerFFT™ / FFTC and drives the four connected memory banks.

The idea is that the application on the LEON processor prepares a sequence of commands, called a 'macro'. This macro contains a number of commands for controlling the PowerFFT™ / FFTC and commands for controlling the Switch Fabric. This macro is loaded (via PCI, AHB and APB) into the Macro Controller and it will be executed after a 'go' command. After the complete sequence is finished, an interrupt will be send to the LEON processor to indicate that the co-processor is ready for a new task.

#### 4. FLEXIBLE BY DESIGN

The OPDP is flexible and powerful in a number of ways.

First, the OPDP can perform a number of different operations at high speed

- The PowerFFT™ / FFTC can perform a 1024 FFT-operations in 10 us. That is FFT-data processing with a speed up to 100 Mcps (Mega complex samples per sec)
- All data paths are 64 bits wide
- Different formats and format conversions are implemented (64 bits floating point, 32+32 integers, signed, etc)
- FFT-operation, Inverse FFT operation, Conjugate operation, Multiplication, Extraction
- 1D FFT-operation and 2D FFT-operation
- Data cross corner turning (id est: write horizontal, read vertical)
- Stepping through the memory banks (for example for filtering)

Second, the OPDP is flexible as with the Switch Fabric different routes can be established. Data input from, for example, the instrument can be routed directly to the PowerFFT™ / FFTC for data processing, but it can also be routed to the SDRAM to establish a continuously data stream. With the Switch Fabric, the output of the PowerFFT™ / FFTC can be routed to an SDRAM for later calculations, or routed via the UserBlock for special (fast) data calculations, or provided to the LEON processor for data calculations.

The OPDP is flexible as it has a UserBlock available in the FPGA for special data calculations that need to be performed at high speed. An example could be a square root operation or finding the optimum in the frequency spectrum (finding resonance frequencies)

The OPDP is modular in its design. Next to the already defined User Block, the OPDP can be extended with additional (mission dependant) interface blocks. In the future fast interfaces like SpaceFibre/WizardLink or GLink can easily be implemented.

Finally, provisions are made to connect multiple OPDP boards to each other, having more than one FFTCs available for even more demanding applications

**5. SPACE QUALIFICATION**

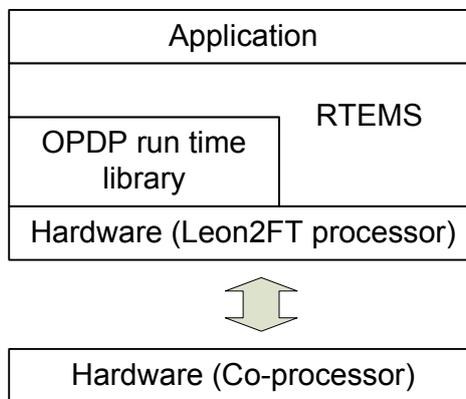
The current breadboard OPDP is based on commercial components. However, the design is completely focused on space qualified components. With the availability of the FFTC (Fast Fourier Transformation Co-processor), which is the space qualified version of the PowerFFT™, an EM and FM model of the OPDP can be developed after this project.

The space qualified version of the OPDP will be a single board, on which the LEON2-FT, the FFTC, the SDRAMs and the FPGA are all implemented on one PCB. Current foreseen size is extended double VME (280 x 233 mm). An overview of the differences is depicted in table 1.

*Table 1. Space qualified components for OPDP*

	<b>OPDP breadboard</b>	<b>OPDP space qualified</b>
Processor	LEON2-FT (Atmel eval board)	LEON2-FT (Atmel)
FFT-chip	PowerFFT™ (Eonic)	FFTC (Atmel)
FPGA	ProAsic3000 (Actel)	RTAX2000S (Actel)
SDRAM memory	K4S513233 (Samsung)	72SD3232 (Maxwell)
Assembly	Processor board plus Co-processor board	One single board
Command & Control	RS232	TBD
Data interfaces	RS232 and SpaceWire	TBD

**6. SOFTWARE / BOARD SUPPORT PACKAGE**



*Fig. 3. Software structure on the LEON processor*

For this project, the RTEMS operating system is selected, but the specific OPDP drivers can be ported to other operating systems, if needed. A run time library is written for the OPDP co-processor board which provides the drivers for each component on the co-processor board. Such as a driver for the Macro Ctrl, the FFTC Ctrl, the Switch Fabric Ctrl, the PCI and the SDRAM memories. The payload application (C or C++) runs under RTEMS and will use the drivers to access the underlying hardware components. See figure 3.

For the application, several default settings are available and different example macros will be provided.

## 7. SOFTWARE DEVELOPMENT ENVIRONMENT

Besides hardware, the Dutch consortium is developing a Software Development Environment (SDE). The objective of the SDE is to provide users with a set of integrated tools for development and testing of mission specific software running on the OPDP board.

The framework is based on Eclipse; the OPDP specific parts are implemented as plug-ins. Some screenshots of the SDE are presented in figure 4. The SDE contains of the following parts:

- Gaisler Build Suite
- Macro Definition tool
- Performance Profiler
- Simulator

The idea of the SDE is that a user can develop the application, debug it, compile and simulate. The final application can be transferred to the real hardware, without modifications. The final behaviour on the real hardware will be very close to the behaviour in the simulation environment.

Key element in the SDE is the definition of the command sequences, called ‘macro’ that controls the PowerFFT™ / FFTC and the Switch Fabric. All different PowerFFT™ / FFTC commands are supported: the different data formats, the 1D and 2D functionality etc etc. It includes the data corner turning functionality. For creating the macros, the user can use a wizard that guides you through the different options and settings. For more experienced users the macro can be edited in the xml-file and converted to the macro bin-format. The macro bin-file will be exactly the same file that is to be used on the real OPDP hardware. Next to the PowerFFT™ / FFTC commands, the commands for the Switch Fabric needs to be determined to establish the different data routes. Also for this part a wizard is available. With the Performance Profiler one can optimize the performance (data throughput) of the PowerFFT™ / FFTC. This to avoid long idle time of this co-processor. Finally, the simulator gives all tools for simulation of the application and simulation of the PowerFFT™ / FFTC behavior.

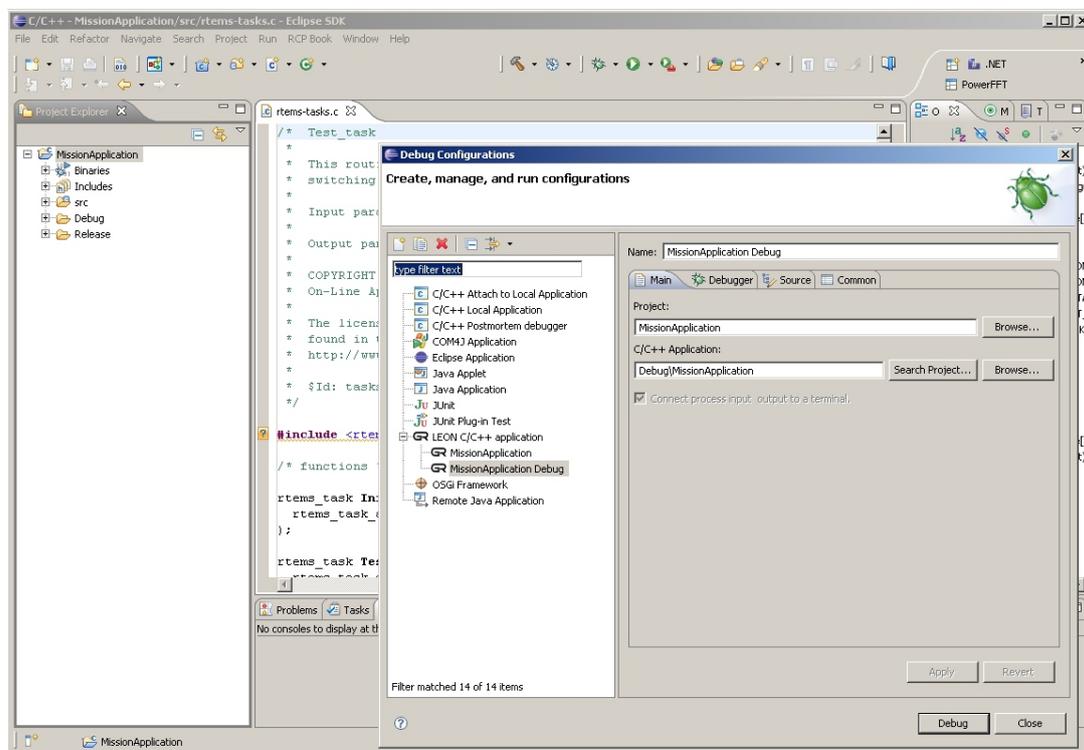


Fig. 4. Screenshot of the LEON application debugger in the SDE (in Eclipse)

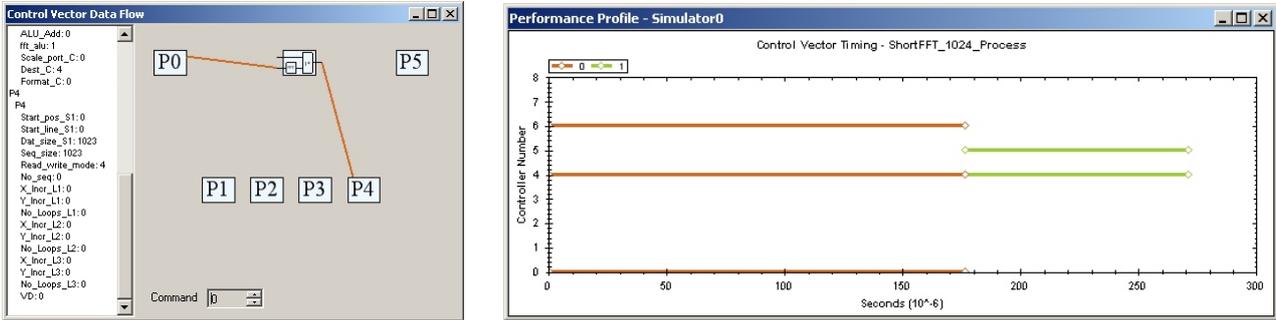


Fig. 5. Screenshots of the Macro Definition tool and the Performance Profiler in the SDE (in Eclipse)

In figure 6. the Simulation structure of the SDE is presented. On top of the PC-hardware and its operating system, the TSIM LEON hardware simulator is used. RTEMS will be running on this TSIM environment; the application will run on RTEMS, just like it will on the real hardware.

In figure 7, an overview of the Simulation part is given. To simulate the payload application on the simulation environment, the TSIM LEON hardware simulator is used. The application will call different macro definitions. On the real hardware, such a macro is a binary file stored on one of the flash memories; in this simulation environment the macro is a bin-file image, stored on the C-drive of the PC. The data interfaces are represented by in- and output files.

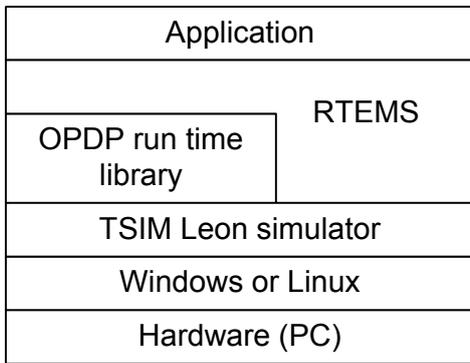


Fig. 6. Simulation software structure of the SDE

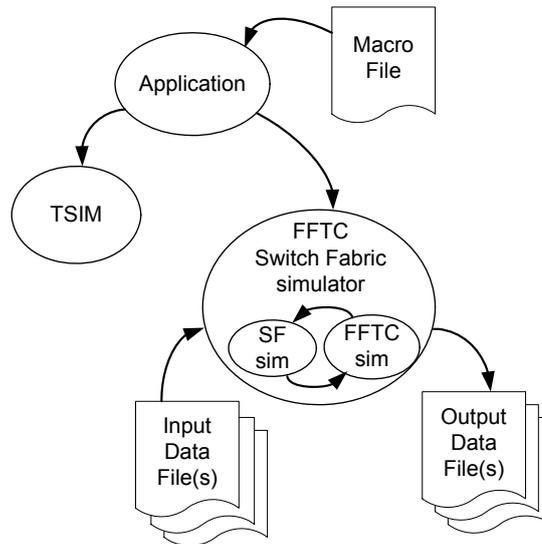
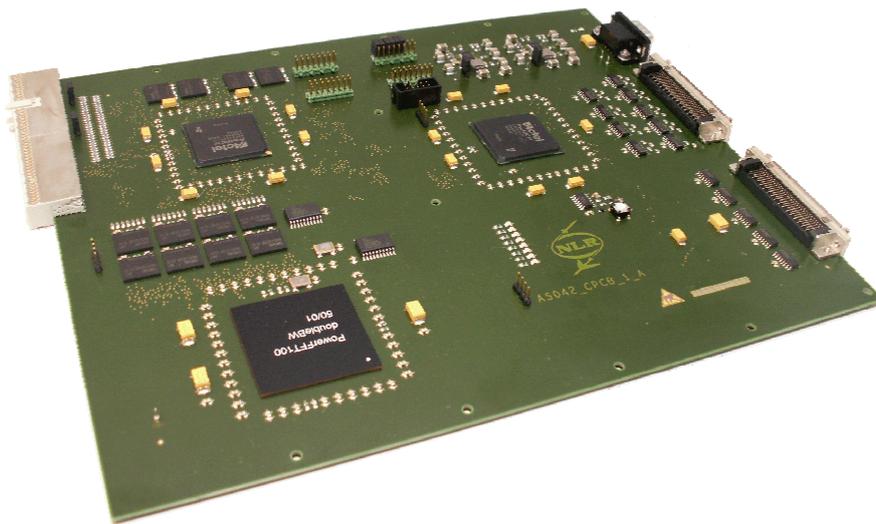


Fig. 7. Simulation part of the SDE for OPDP

## 8. CONCLUSIONS

- OPDP is a complete “full package solution”
- OPDP combines the power of the FFTC co-processor with the flexibility of the LEON2-FT processor
- OPDP will establish a data throughput of 95 Mcps (Mega complex samples per second)
- OPDP incorporates all possible FFT-operations of the FFTC / PowerFFT™
- OPDP has a Software Development Environment in which the user can develop the application, debug it, compile and simulate. The final behavior on the real hardware will be very close to the behavior in the simulation environment.
- OPDP is based on RTEMS but portable to other operating systems

With this development, OPDP can accommodate any satellite that needs data processing with high speed FFT-operations. Especially SAR satellites, but also altimeter missions and spectrometry instruments and even SWIR satellites could highly benefit from this fast FFT-oriented processing capabilities. Space qualification is within reach.



*Fig. 6. Picture of the developed OPDP co-processor board*

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