Nationaal Lucht- en Ruimtevaartlaboratorium

National Aerospace Laboratory NLR

Executive summary

Frequency Domain SAR Data Compressor

Problem area
Advanced multi-mode SAR instruments such as the main instrument of the Sentinel-1 Earth Observation satellite require high-performance on-board data compression. Conventional solutions can not meet these requirements. This calls for new approaches using advanced space-qualified ASIC devices.

Description of work
In this paper a novel approach to the on-board compression of raw SAR data is presented. The so-called Entropy-Constrained Block Adaptive Quantization (ECBAQ) algorithm is applied in the frequency domain. Using optimized two-dimensional bit allocation with a carefully designed rate control loop in combination with efficient entropy coding, a design has been achieved that is compatible with the multi-mode operations of the SAR

and that meets the image quality and data rate requirements.

Results and conclusions
For the compression of raw data from multi-mode SAR instruments, Entropy Constrained Block Adaptive Quantization is an attractive option. In particular, in a frequency-domain configuration, the average compression ratio is significantly higher than with conventional systems. The implementation on-board of satellites is feasible due to the availability of the PowerFFT, a very fast FFT-oriented DSP ASIC, which is currently being space-qualified.

Applicability
The presented compression method is an attractive compression method for application on all future SAR satellites.

NLR-TP-2008-393

Frequency Domain SAR Data Compressor

T. Algra and G.J. Vollmuller

This report is based on a presentation at the On-Board Payload Data Compression Workshop OBPDC 2008, ESA/ESTEC Noordwijk, 26-27 June 2008.

The contents of this report may be cited on condition that full credit is given to NLR and the authors.

This publication has been refereed by the Advisory Committee AEROSPACE SYSTEMS & APPLICATIONS.

Contents

Abbreviations

ASIC	Application Specific Integrated Circuit
BAQ	Block Adaptive Quantization
CCSDS	Consultative Committee for Space Data Systems
DSP	Digital Signal Processor
ECBAQ	Entropy Constrained Block Adaptive Quantization
EW	Extra Wide swath
FDBAQ	Flexible Dynamic Block Adaptive Quantization
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FFTC	FFT Co-processor
FPGA	Field Programmable Gate Array
IP	Intellectual Property
ISLR	Integrated Side Lobe Ratio
LUT	Look-Up Table
MIPS	Million Instructions Per Second
PSLR	Peak Side Lobe Ratio
SAR	Synthetic Aperture Radar
SDRAM	Synchronous Dynamic Random Access Memory
SLC	Single Look Complex
SQNR	Signal to Quantization Noise Ratio
SRAM	Static Random Access Memory
VHDL	VHSIC Hardware Definition Language

FREQUENCY DOMAIN SAR DATA COMPRESSOR

Theo Algra, Bert Johan Vollmuller

National Aerospace Laboratory NLR,
P box 90502, 1006 BM Amsterdam,
The Netherlands,
Email : algra@nlr.nl

ABSTRACT

This paper presents a frequency-domain SAR data compressor which outperforms the conventionally used Block Adaptive Quantization (BAQ) compressor. For advanced multi-mode satellite SAR instruments, such as the one to be implemented on-board of Sentinel-1, the average compression ratio can be significantly increased as compared to BAQ. Space borne implementation with a high-speed data throughput is feasible due to the advent of advanced space FPGA's and ASIC's including the powerFFT, a fast FFT-oriented DSP. The complete compressor module can be implemented on an extended double size Eurocard.

1   INTRODUCTION

SAR sensors on-board of remote sensing satellites such as Sentinel-1 generate increasing amounts of data. However, due to download data budget limits, the number of scenes that can be acquired is constrained. This calls for the application of on-board data compression.

Block Adaptive Quantization (BAQ) has been applied in a number of space SAR systems, but this method has a moderate compression ratio. Until today the rapid developments in terrestrial compression technology of the last decade(s) have not yet resulted in substantial improvements of on-board SAR data compression systems. This was mainly due to the lack of suitable space-qualified and ultra-complex ASIC's as well as the specific properties of raw SAR data.

This paper presents a new-generation SAR data compressor intended for application on SAR satellites such as Sentinel-1. A high-performance compression method has been developed that operates in the frequency-domain. The FFT-ECBAQ algorithm (Fast Fourier Transform- Entropy Constrained Block Adaptive Quantization) can perform on-the-fly compression with a high-speed data throughput, using an efficient architecture that is based on the fastest space-qualified FPGA and DSP ASIC's available today. One of the key building blocks is the PowerFFT ASIC, currently the fastest DSP for FFT operations. This ASIC will become available in a space-qualified version and its application allows an efficient implementation of the FFT-ECBAQ algorithm involving two-dimensional FFT operation.

The paper successively describes the compression method, the powerFFT device, the design of the compressor, the development and test approach, and the simulation performance results. Currently, under ESA contract, a breadboard version is being developed, with compression ratio and data throughput fully compatible with Sentinel-1 requirements.

2   EFFICIENT ON-BOARD SAR DATA COMPRESSION

The data compressor consists of four main elements (Fig. 1). The input data stream comprises alternating I and Q samples of 10 bits, with a maximal average rate of ~160 Msamples/s. The Pre-processing and 2D-FFT stage transforms the complex input data to the frequency domain. Second, the ECBAQ function performs the actual compression. Third, the encoded data is packed into a CCSDS-compatible source format. Finally the Control & Timing element provides timing and telemetry signals and allows controlling the compressor by external (tele)commands.

2.1 ECBAQ

ECBAQ [1] divides the input data into blocks of, for example, 128 samples, which is similar to BAQ. The digital numbers are multiplied by a scaling factor and then uniformly quantized. The step size is smaller than in the case of
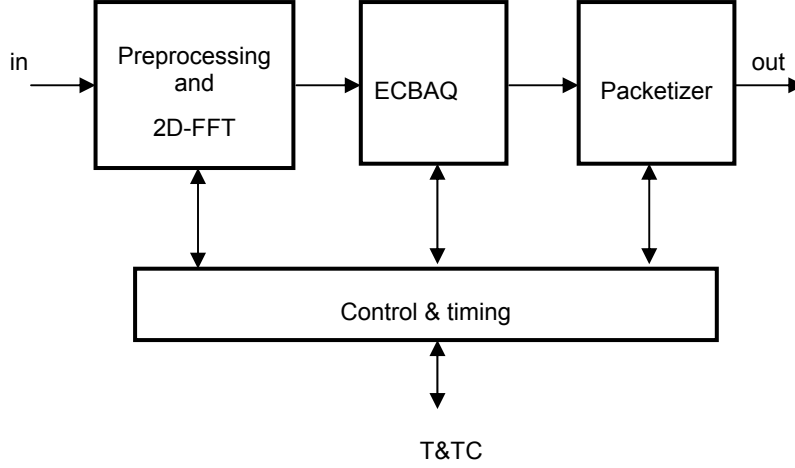
Fig. 1   FFTECBAQ Block diagram

BAQ and the range is larger. After quantization, a variable-length encoder, for example a Modified Huffman encoder, compresses the data, after which the bit stream chops the data into 16-bits words. After each block, the rate control updates the scaling factor. It is possible to accumulate the encoded word lengths and calculate the average coding rate of the completed block. Comparing this actual coding rate with the required rate, the scaling factor can be increased, decreased, or left unchanged.

In [2,3] an ECBAQ design has been presented with another rate control loop mechanism, which is also suitable to frequency-domain operation. The parameter used by the rate control loop is not the average coding rate, but the counted number of samples with absolute value smaller than a reference standard deviation (σ_{REF}). It can be assumed that the clutter signal has a Gaussian probability density function. Hence the counted number of samples with absolute value < σ_{REF} is directly related to the current standard deviation. Refer to figure 2.

Let C_L be the total number of absolute values < σ_{REF} within a block of M consecutive samples. Then

$$\overline{C_L} = M \int_0^{\sigma_{REF}} \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-0.5(x/\sigma)^2\right] dx \tag{1}$$

At the block transition moment, C_L is compared with a lower and an upper limit to decide whether the step size S has to be increased or decreased:

$$S_{k+1} = S_k / D \qquad if \ C_L / M > \Delta_1$$

$$S_{k+1} = S_k * D \qquad if \ C_L / M < \Delta_2 \tag{2}$$

D is a constant. $D = 1.41$ (3 dB) gives good performance results. The limits Δ_1 and Δ_2 correspond to distributions with $\sigma = \sigma_{REF} + 1.5$ dB and $\sigma = \sigma_{REF} - 1.5$ dB , respectively,

$$\Delta_1 = \int_0^{\sigma_{REF}} \frac{1}{\sigma_{REF}\sqrt{2\pi / D}} \exp(-0.5(\frac{x\sqrt{D}}{\sigma_{REF}})^2) dx$$

$$\Delta_2 = \int_0^{\sigma_{REF}} \frac{1}{\sigma_{REF}\sqrt{2\pi D}} \exp(-0.5(\frac{x}{\sigma_{REF}\sqrt{D}})^2) dx \tag{3}$$

Note that the step size changes are derived from the quantized values. Hence the decoder can perform the same operation and it is not necessary to multiplex the standard deviation codes into the codeword stream as is done with BAQ. The quantizer output is efficiently entropy-coded using a Modified Huffman scheme. This means that with an almost negligible performance loss, the maximum code word length will be limited to a practical length of 16 bits.

The Signal to Quantization Noise Ratio (SQNR) of ECBAQ with such a rate control loop exceeds the SQNR of BAQ by 2.2 dB at 4 bits/sample [2]. Moreover, ECBAQ allows non-integer bit rates [1]. Some other advantages of this version of ECBAQ are: there is no block buffer needed; the instantaneous dynamic range can be large; the performance of the control loop is independent of the implemented entropy code.
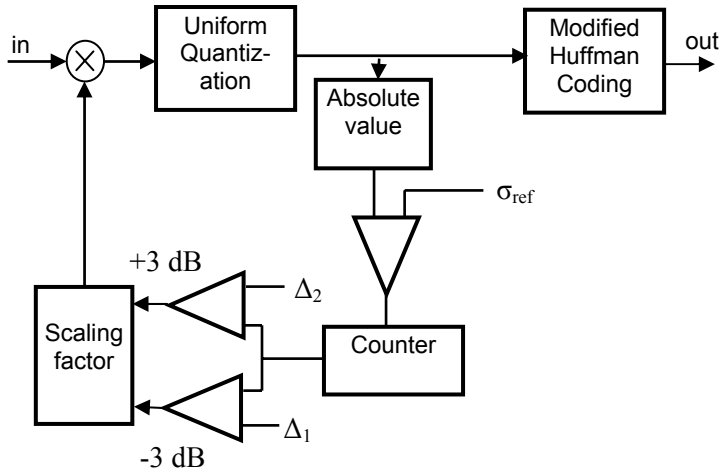
Fig. 2 ECBAQ Block diagram

2.2 Frequency-domain ECBAQ

Substantial higher compression ratios can be achieved when the ECBAQ operates in the frequency domain. In the digitization section of a SAR system always oversampling is applied in the range dimension. Moreover, also in the azimuth dimension oversampling is commonly applied due to the fact that the Doppler processing bandwidth should be significantly smaller than the Pulse Repetition Frequency in order to achieve a sufficient level of image quality. These oversampling factors usually depend on the SAR mode and the subswath and may range from 15% to more than 50%. Consequently, after 2D-FFT transformation, the coefficients which correspond to these oversampling regions can be quantized more coarsely i.e. with a lower bit rate than the other ones.

For speed and memory size reasons the FFT size is limited in practical implementations. In azimuth a 64-points complex FFT is used and in range a 128-points complex FFT. Without the application of overlap & save/add method - which would lead to lower compression gain - these relatively short sizes will cause some cross leak noise when the data of the oversampling regions would be entirely omitted, i.e. not encoded and transmitted at all.

The compression ratio can be further optimized by applying frequency-dependent quantization taking into account the application of apodization functions in SAR image formation processing in the ground segment. In other words, for
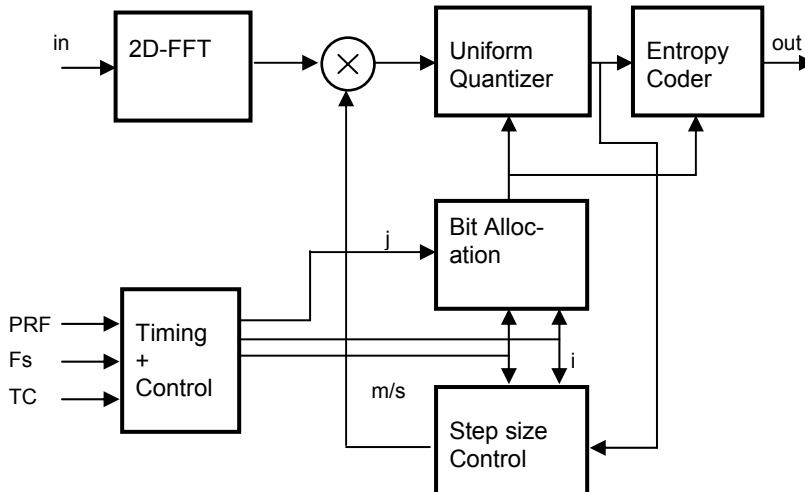
Fig. 3 FFTECBAQ Block diagram

each of the 128 x 64 complex coefficients in the 2D-FFT output block a particular optimal step size is applied with an associated bit rate.

Although the probability density function of the quantization input approximates a Gaussian distribution, the signal includes high peaks due to bright scatterers. This requires a significant extension of the instantaneous dynamic range. Therefore in this ECBAQ design 4096 quantizer output levels have been implemented to ensure sufficient instantaneous dynamic range without noticeable performance loss.

The use of the rate control loop has several advantages here: i) the scaling factor values do not have to be transmitted; ii) there is no need for a block buffer of 128 complex samples; iii) more important, the loop serves as a low pass filter for the scaling factor updates, suppressing spurious deviations due to high peaks.

The compressor includes a bit allocation matrix (128 x 64) for each of the possible mode/subswath combinations of the SAR instrument. Fig. 4 shows an example.

Due to the fact that the adopted method of rate control almost only depends on the clutter statistics, the scaling factors are less influenced by large signal peaks due to bright point scatterers. This is an essential and indispensable property of the presented design.

Usually the signal level in the range oversampling band is relatively low, as compared to the signal band. Therefore in the range oversampling area of the FFT domain, run length coding is applied in addition to the Huffman coding.

Note that in a number of the Sentinel-1 SAR modes, the Doppler Centroid is continuously changing during the burst. The encoder compensates this before the FFT operation as will be explained in section 4.
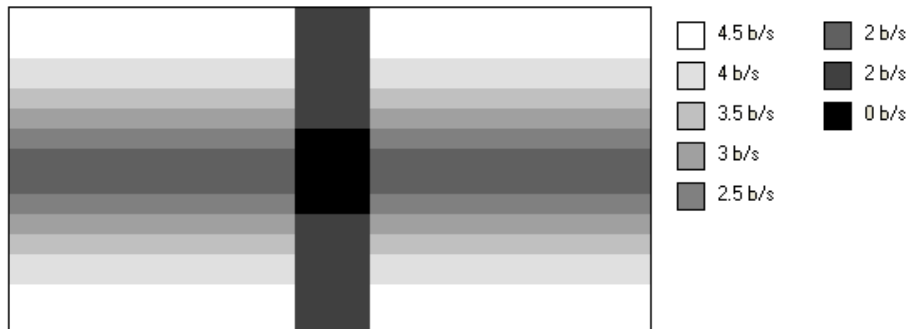

Fig. 4   Example of a bit allocation matrix (128 x 64 complex coefficients)

3   FFT CO-PROCESSOR ASIC

Available space-qualified DSP based modules offer a typical computing power of 20 MIPS and more noticeably 20 MFLOPS to 60 MFLOPS. Although it was considered as high a few years ago, future space applications like raw SAR data compression, radar altimeter processing, optical image processing and even on-board SAR image generation, require a much higher computing power while keeping a substantial level of configurability and flexibility. Therefore a solution based on a specialised processor was favoured by ESA for space applications, the so-called "Fast Fourier Transform Co-Processor" (FFTC).

The design of the FFTC is based on the commercially available PowerFFT™ processor IP licensed by ESA from Eonic B.V.[4]. The PowerFFT is the world's fastest and most powerful programmable FFT-centric floating-point DSP, able to process 100 million complex samples per second in continuous mode, with a rich set of functionalities for Fast-Fourier Transforms (FFT) computations and FFT-based algorithms, including N-dimensional FFTs, correlations and convolutions. The PowerFFT is a mature ASIC, implemented in numerous military and commercial applications.

The PowerFFT has a 64 bit primary input port, 64 bit primary output port and can execute up to 1K pts FFT or convolution, including windowing, sustained in 10 µs with floating point precision. Four additional I/O ports are available for 4 optional SDRAM (or SRAM) bank extensions for long FFTs, FFT based multi-dimensional algorithms, overlapped algorithms, and (double buffered) corner turning operations.

The flexibility of the memory bank type is guaranteed by using an Address Generator FPGA, which allows cost-effective memory use, easy adoption to addressing schemes, easy upgrades to larger memories, and specialized memory use for space and military applications. A standard instruction set for the PowerFFT is available for FFT macro-

functions (≤ 1M pts. 1D FFT / convolution / correlation, ≤ 1K × 1K pts. 2D FFT / convolution / correlation). Upgrade instruction sets can be developed for large (> 1M pts.) 1D, (>1K × 1K pts.) 2D and multi-dimensional FFT-based algorithms (user specific), and other FFT-like Fast Transforms such as Chirped-Z Transform (CZT).

The PowerFFT supports the following standard data formats:

- 32 bit IEEE floating point (parallel or sequential I&Q);
- 32 or 16 bit integer (parallel or sequential I&Q);

And the following specialized data formats:

- 16 or 32 bit sign inverted integer (parallel and sequential I&Q);
- 2×24+9 bits hybrid floating point;
- 2×12+8 bits hybrid floating point.

The PowerFFT runs on a 100 MHz I/O clock maximum, and a 128 MHz internal processing clock.

Currently ESA is developing a radiation tolerant version of the PowerFFT and plans to make this FFTC device available to European industry as an ASSP (Application Specific Standard Product) in the course of 2009.

input I,Q

Preprocessing and i/f FPGA

Command, Telemetry, Timing and Control

De-offset
DC compensation

Memory Control

Alternating buffer
2 x 64 range lines

64 p Azimuth FFT

128 p Range FFT
Scaling
Output in 16 b integer

C/M →

Alternating buffer
2 x 128c x 64

Multiplication

Quantization

Rate Control

Bit allocation

rate

I   M/S   C/M

Modified Huffman coding
&
Run-length coding

M/S   I   J   C/M

Word Forming
FEC coding

M/S = mode/swath identifier
C/M = compression mode
I = range line index Modulo 64
J = range sample index Modulo 128

C/M →

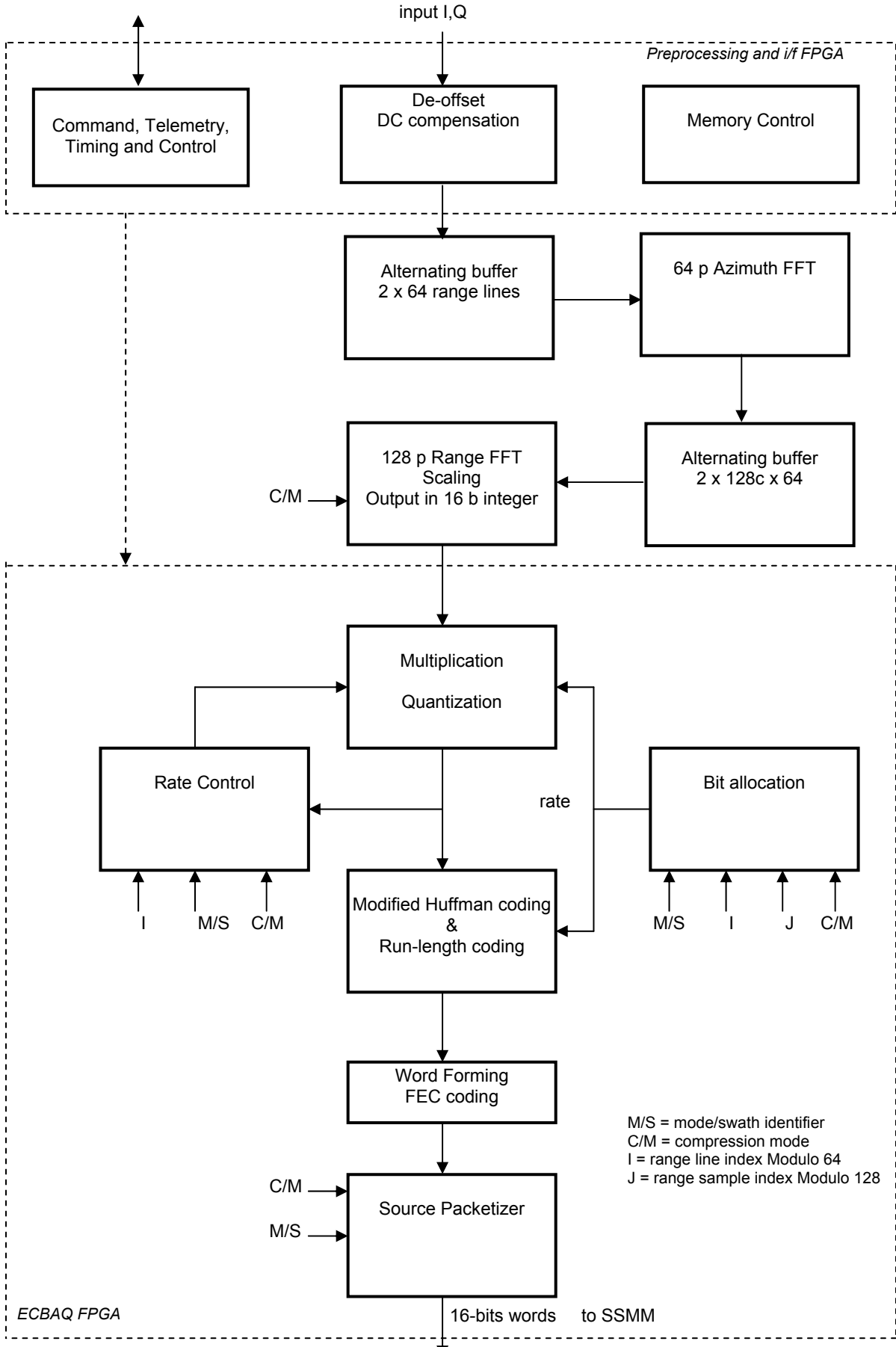Source Packetizer

M/S →

ECBAQ FPGA

16-bits words   to SSMM

Fig. 5 System diagram

4 COMPRESSOR ARCHITECTURE

Fig. 5 shows the system diagram. The pre-processing & interfacing FPGA performs the following functions:
- Echo line buffering to reduce the peak input rate
- Number format conversion (De-offsetting)
- Doppler Centroid compensation (in some modes)
- Memory control for the FFT stage
- Board timing signals generation
- System interface for telemetry and command

The FFT stage uses two powerFFT devices. The first one performs 64 complex points azimuth the second one 128 complex points range FFT. This 2-dimensional operation requires corner turning of the data. This is accomplished by an alternating buffer of 2 x 64 range lines and a total size of 16 MB.

The ECBAQ FPGA processes the output of the second powerFFT, consisting of 32-bits complex 2D FFT coefficients, each with a real and an imaginary part.

For the ECBAQ FPGA architecture the following design constraints have been taken into account:
1- The design shall be flexible and upgradeable;
2- Minimize the size of memory resources (LUTs) as much as possible to avoid the necessity of external memory components;
3- Effectively the maximum input throughput shall be up to 160 MSPS, but higher throughputs shall be possible in the future.

This FPGA performs the following functions:
- Adaptive Quantization according two-dimensional variable bit allocation
- Entropy coding (Modified Huffman followed by run-length)
- Rate control
- Variable-length to Fixed-length conversion (16 bits words)
- 2-dimensional parity coding for additional protection against transmission bit errors
- Source packetizing

Note that the bit allocation and rate control tables are SAR mode and subswath dependent. The encoded data of each 2D FFT block results in a self-contained CCSDS source packet. In other words each packet can completely be decoded without the need for information from previous packets. The FFT-ECBAQ is able to switch to time-domain compression. In that case the FFT stage is bypassed and the ECBAQ algorithm is performed in the time-domain.

The parity coding function provides additional protection against transmission bit errors. Although the probability of a bit error is small (10^{-9}), the effect may be that a (large) part of 128x64 samples block is erroneously decoded due to the loss of synchronization in the variable-length coding stream. With parity coding the resulting bit error probability is reduced to less than 10^{-11} at the expense of about 1% coding rate increase.

The ECBAQ implementation fits in a medium-sized space qualified FPGA (Actel RTAX2000). The complete compressor module can be implemented on an extended double size Eurocard. The output data is directly relayed to the on-board mass memory using high speed data links.

In some SAR modes, such as Interferometric Wide swath (Sentinel-1), a form of progressive beam scanning is applied. During the burst, the squint angle linearly changes from a negative to a positive value. Consequently the Doppler Centroid varies also, with a rate of a few kHz/s. However, in order to apply 2D FFTECBAQ, we need a constant value of the Doppler Centroid in order to apply correct bit allocation in the azimuth direction. Therefore a frequency shift is applied on the raw data, in the encoder, resulting in zero Doppler. The operation is exactly reversed in the FFTECBAQ decoder. The Doppler Centroid compensation can be implemented by adding a phase value to each complex sample according to equation (4):

$$\Phi(i, j) = C(A + i)(B + j)i \qquad (4)$$

Here A, B, and C are constants dependent on the sub swath and mode; i is the range line number of the burst; j is the range bin.

The Doppler Centroid compensation is performed by the preprocessing FPGA.

The flight version of the encoder will be equipped with provisions to allow in-flight updating of bit allocation tables and Doppler Centroid compensation parameters.

4 DEVELOPMENT AND TEST APPROACH

Fig. 6 shows the basic test setup. The encoder is tested with real and synthetic raw SAR data. The original data as well as the decompressed data is processed into single-look complex slant-range images with equal processing parameters. The two images are compared to derive the compression noise level and to evaluate the image quality. The development comprises the following phases.

First a software-based encoder/decoder pair is developed and tested against the specifications. Image quality, compression ratio, and estimated on-board data speed are the verification requirements. In the next phase the ECBAQ part of the encoder is replaced by a VHDL simulation of the ECBAQ FPGA. Finally, the software encoder is completely replaced by the hardware model.

The test setup includes a feature to generate random bit errors in the compressed data in order to verify the built-in error correction mechanism.

5 PERFORMANCE

Extensive simulations have been performed with real and synthetic SAR data [2, 5]. It has been demonstrated that FFTECBAQ results in excellent SAR image quality. Resolution, PSLR, and ISLR are not influenced by the coding process. Figure 7 shows the resulting coding rates for the various Sentinel-1 SAR modes as well as ERS, with an average signal to quantization noise ratio ≥ 21 dB in the single-look complex slant-range image. It should be noted that in the Sentinel-1 digitization chain sub-sampling will be applied in range direction. This data reduction step minimizes the range oversampling factor. Otherwise the FFTECBAQ coding rates would be even significantly lower.
Notes:
- For the Extra Wide swath mode (EW) one-dimensional FFTECBAQ has been used in the simulations
- All the rates include forward error correction codes
- Scenes with a lot of bright scatterers will show a slight increase of the coding rate along with a higher SQNR
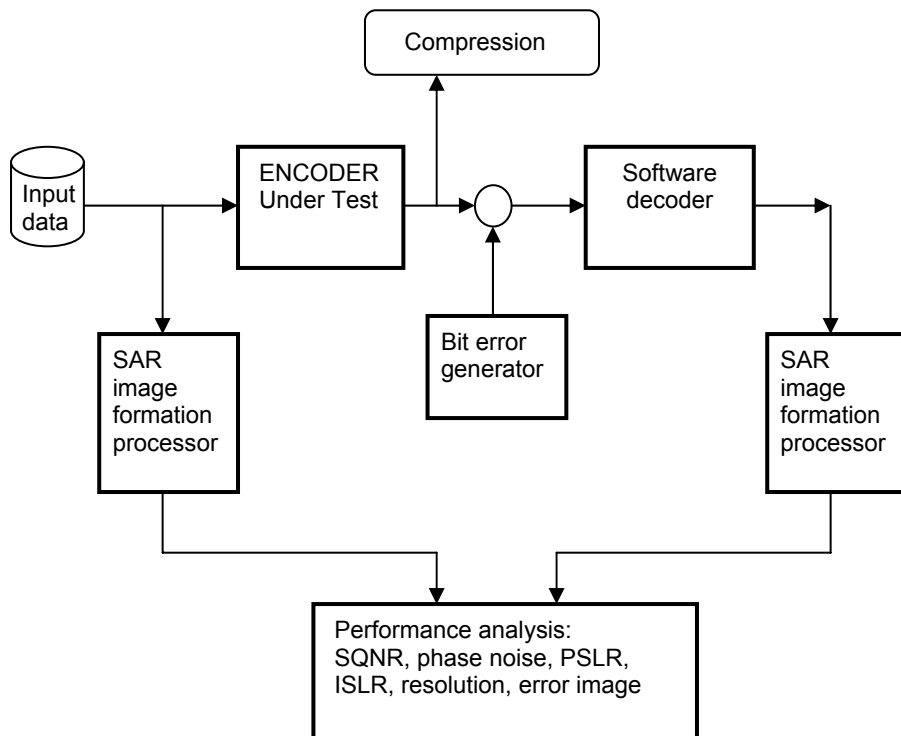

Fig. 6 Test approach

6   CONCLUSIONS AND RECOMMENDATIONS

For the compression of raw data from multi-mode SAR instruments, FFTECBAQ (frequency-domain Entropy-Constrained Block Adaptive Quantization) is an attractive option. The achievable compression ratio is substantially higher than with BAQ. The implementation on-board of satellites is feasible due to the availability of the PowerFFT, a fast FFT-oriented DSP ASIC, which is currently being space-qualified.

Additional data reduction can be achieved with a varying, scene-dependent, target SQNR level [6]. Basically, the FFTECBAQ design already includes the building blocks for such a function. Therefore it is recommended to investigate the feasibility of this option.
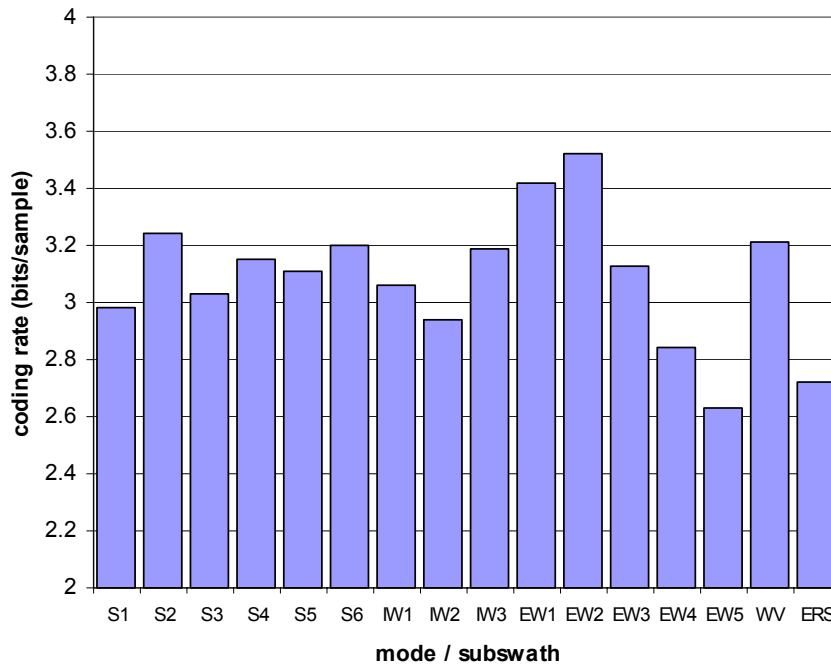

Fig. 7   Performance results (SQNR = 21 dB in SLC image)

7   REFERENCES

[1]   Algra, T., Compression of raw SAR data using Entropy-Constrained Quantization", Proc. IGARSS, Honolulu, 2000

[2]   Algra, T., L. Bierens, Advanced on-board SAR data compression FFT-ECBAQ performance and quality test results, NLR-CR-2006-87, ESA contract 18992/05/NL/MV, 2006

[3]   Algra, T., L. Bierens, Enhanced SAR data compressor for Sentinel-1, Proc. DASIA, Naples, 2006

[4]   PowerFFT Data Sheet, EONIC B.V., Delft

[5]   Algra, T., Preliminary Simulation Results Frequency Domain raw SAR Data Compressor, NLR-CR-2007-865, ESA contract 21055/07/NL/LvH, Amsterdam, 2008

[6]   Rizzoli, P., Attema, E., et al, FDBAQ Performances Analysis for C-Band SAR Sensor, On-Board Payload Data Compression Workshop - OBPDC 2008, Noordwijk, June 2008