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On-board FFT Data Processing for GNSS Reflectometry

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Executive summary

On-board FFT Data Processing for GNSS Reflectometry

Problem area
Recently, GNSS reflectometry (GNSS-R) has become popular as a powerful remote sensing technique for observing ocean altimetry, sea state and soil moisture.
With some 150 GNSS satellites to be available in the near future, the use of GNSS signals for novel sensing applications, like GNSS-R, are possible. GNSS-R missions demonstrating this type of technology are currently under development. Fast processing power is needed to be able to process this type of data in real-time, avoiding the storage of large amounts of data on the satellite and downloading this data to the ground segment.
The Fast Fourier Transform (FFT) has been demonstrated to be a computational efficient approach for GNSS signal processing.
In this contribution, a space qualified Data Processing unit, based on FFT-processing, is introduced that could enable the full potential of GNSS-R.

Description of work
For GNSS based navigation, signal acquisition has to be performed when the receiver is switched on over a range of Doppler shifts and code phases and -if the user and/or GNSS satellites positions are unknown- for all GNSS satellites. The sequential search is widely used in GNSS receivers for signal acquisition as it is straight forward to implement, however it is computational expensive.
The FFT has been demonstrated to be a more computational efficient approach for acquisition, but has not yet been applied for spaceborne GNSS applications.
A GNSS-R payload consists of two antennas: one antenna is zenith pointing and the other is nadir pointing. The reflected signals are affected by reflector's surface "roughness", motion, mean surface height and dielectric properties.
For processing the GNSS-signal onboard a spacecraft, one could choose a space qualified microprocessor. The drawback is that space qualified processors are not very fast and therefore the on-board processing will take several minutes for even the shortest data set. Faster on-board processing could be achieved with an implementation in VHDL in a space qualified FPGA. In theory this method can give a very fast processing if all processes can be performed in parallel. However, this is in practice not possible due to the limited FPGA resources that are available.

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This report is based on a presentation held at the ION International Technical Meeting, San Diego, California, January 28-30, 2013.

Revolutionary is the solution with the use of a fast space qualified FFT-coprocessor: the FFTC. NLR has developed a Data Processing board, coined the On-board Payload Data Processing (OPDP), based on a FFTC ASIC that is developed under ESA license and available since early 2012. This chip, a rad-hard ASIC in the 0.18µ process of Atmel, can be regarded to be the fasted space qualified FFT-coprocessor in the world.
OPDP consists of three boards and a backplane:
a) A LEON-board for general purpose processing and instrument control;
b) An FFTC-board for high-performance instrument data processing;
c) An I/F-board with WizardLink I/O for high-speed interfacing and pre-processing of instrument data;
d) A passive backplane with high-speed data interconnect and power distribution.
The three boards give an extensive set of data processing capabilities, but with this modular setup and the open (backplane) interfaces of OPDP, the end customer gets many possibilities to adjust the OPDP concept to its own on-board data processing needs.
In this contribution, we have tested the applicability of this Data Processing board for spaceborne GNSS applications.

Results and conclusions
GNSS reflectometry could become a powerful remote sensing technique for earth observation satellites. Fast processing power is desirable to process the GNSS data in real-time, avoiding the storage of large amounts of data on the satellite and downloading this data to the ground segment. The FFT has been demonstrated to be a computational efficient approach for GNSS signal processing.
This paper presented a detailed description of a space qualified FFT-Coprocessor unit and it's potential for spaceborne GNSS applications including GNSS-R. Moreover, the co-processor could be utilized for fast GNSS signal acquisition after power on of a GNSS receiver and for reacquisition of the GNSS signals after a latch-up which could occur due to radiation in the space environment.

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On-board FFT Data Processing for GNSS Reflectometry

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BIOGRAPHIES

Peter Buist is a Senior R&D Engineer at the National Aerospace Laboratory NLR. He worked in the Japanese aerospace industry for 8 years, specializing in particular in Global Navigation Satellite System (GNSS). In Japan, he developed GPS receivers for the –among others- Japanese SERVIS-1, USERS, ALOS satellites and the H2A rocket. His research interest includes all expects of navigation and (onboard) data processing.

Bert-Johan Vollmuller is Project Manager of the On-board Payload Data Processing module and currently responsible for the design and manufacturing of the E(Q)M. In the past Bert-Johan was involved in many satellite electronics projects: project manager of a Mass Storage Device (currently installed in the ISS), main electrical engineer of Sloshsat (a small satellite of 100kg for the verification of computational fluid dynamics), several SAR-related study projects and processor cards for CubeSats.

ABSTRACT

GNSS reflectometry (GNSS-R) could become a powerful remote sensing technique for earth observation satellites. Fast processing power is desirable to process the GNSS data in real-time, avoiding the storage of large amounts of data on the satellite and downloading this data to the ground segment. The FFT has been demonstrated to be a computational efficient approach for GNSS signal processing.

The paper will present a detailed description of a space qualified FFT-Coprocessor (FFTC) unit and it's potential for spaceborne GNSS applications, including GNSS-R.

INTRODUCTION

Recently, GNSS reflectometry (GNSS-R), which idea was first introduced by Martin-Neira in 1993 [1], has become popular as a powerful remote sensing technique for observing ocean altimetry, sea state and soil moisture.

With some 150 GNSS satellites to be available in the near future, the use of GNSS signals for novel sensing applications, like GNSS-R, are possible. Fast processing power is needed to be able to process this type of data in real-time, avoiding the storage of large amounts of data on the satellite and downloading this data to the ground segment.

In this contribution, a space qualified Data Processing unit, based on Fast Fourier Transform (FFT)-processing, is introduced that could enable the full potential of GNSS-R.

GNSS SIGNAL ACQUISITION

For GNSS based navigation, signal acquisition has to be performed when the receiver is switched on -and if the user position is unknown- over a range of Doppler shifts and code phases for all GNSS satellites. The received GNSS signals are acquired and tracked in the receiver, the obtained messages are decoded and both are utilized to determine the position of the user. The sequential search is widely used in GNSS receivers for signal acquisition as it is straight forward to implement, however it is computational expensive, especially if one would like to increase the integration time for weak signal detection.

For spaceborne receivers this process can be time consuming compared to terrestrial receivers, in particular for receivers based on space qualified components [2][3], but -due to larger Doppler uncertainty- also for receivers using COTS components [4][5]. In space, radiation event (latch-up) could occur. After detection of latch-up, the normal recovery is to restart the receiver, requiring reacquisition of the signals.

The FFT has been demonstrated to be a computational efficient approach for GNSS signal acquisition [6], but has not yet been applied for spaceborne GNSS applications.

GNSS-R MISSIONS

The UK-DMC satellite [7] – launched in 2003 – has demonstrated GNSS-R by collecting reflected GPS data in orbit. In this experiment, sampled IF data was collected on-board with a data recorder and downloaded for post processing on the ground. Typically at most 20 seconds of data was obtained using this approach, enabling the demonstration of the feasibility of GNSS-R but not enough data was obtained to assess the accuracy of this remote sensing technique. An evolution of the UK-DMC payload, the Sea State Payload (SSP), will be launched on TechDemoSat-1 in 2013.

The Cyclone Global Navigation Satellite System (CYGNSS) of NASA – to be launched in 2017 – will enable scientists to investigate the air-sea interaction processes that take place near the inner core of storms, which play an important role in the creation of hurricanes. The eight micro-satellites of CYGNSS will observe the reflected GPS signals providing information on the ocean surface roughness from which wind speed is retrieved.

The PARIS In-Orbit Demonstrator mission is under development at ESA. The instrument features the correlation between the direct and reflected GNSS signals received through high gain, beam-steering antennas in order to measure sea surface heights.

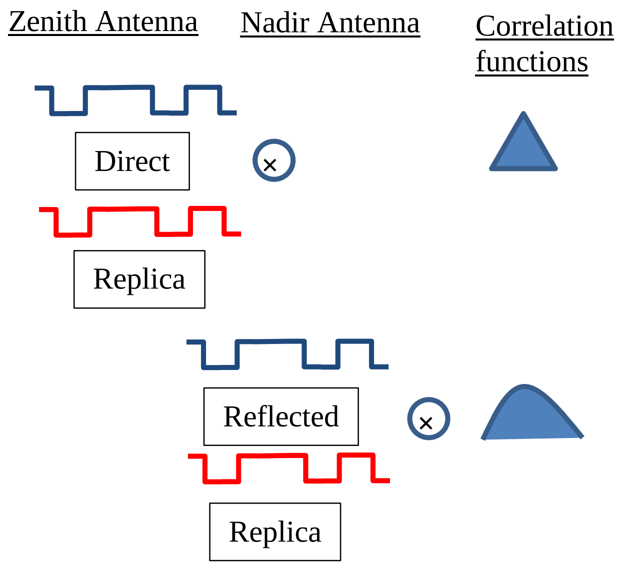

Fig. 1. Conventional GNSS-R Approach

It will make use of a deployable, active double-faced array as antenna, each face comprising 31 dual frequency (GPS L1/ Galileo E1 and GPS L5/ GALILEO E5) elements [8]. Other GNSS-R experiments under development are GORS and G-REX in Germany, PAU in Spain[9], and TriG at JPL.

GNSS-R PAYLOAD

A GNSS-R payload, based on a conventional GNSS receiver design, consists of two antennas: one antenna is zenith pointing (receiving the direct signal) and the other is nadir pointing (receiving the reflected signal). The second antenna has a large aperture to receive the weaker reflected signals and – as the reflection will change the polarization of the signal – is of left-hand circular polarization (LHCP).

The *conventional* GNSS-R payload will generate replicas of the PRN codes for both the direct and reflected signals. Typically, three correlators are used for the direct signal: one at the prompt and the other two located symmetrically early and late with respect to the prompt, resulting in a typical triangular shape of the correlation function.

The reflected signals are affected by reflector's surface "roughness", motion, mean surface height and dielectric properties. Different than the direct signal, the reflected signal has a distorted shape.

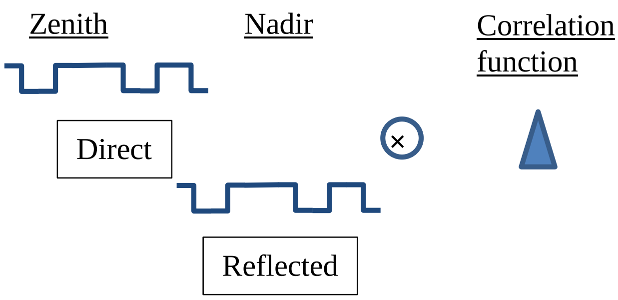

Fig. 2. PARIS Approach

Figure 1 shows both the direct and the (distorted) reflected signal.

The disadvantage of the conventional implementation is that the other signals modulated on the GNSS signals (i.e. for GPS the military P(Y) and M-codes, messages) are not present on the replicas, which will have a negative influence on the correlation between the received signals and replicas.

This disadvantage can be overcome by the Passive Reflectometry and Interferometry System (PARIS) approach in which no replica signal is generated to correlate with the received signals. Instead the received direct and reflected signals are directly correlated with each other (see figure 2).

In the PARIS approach a replica code is still necessary to enable navigation using the direct signal (if required by the mission).

ONBOARD DATA PROCESSING

For processing the GNSS-signal, one could choose a space qualified microprocessor. The drawback is that space qualified processors are not very fast and therefore the on-board processing will take several minutes for even the shortest data set. Faster on-board processing could be achieved with an implementation in VHDL in a space qualified FPGA. In theory this method can give a very fast processing if all processes can be performed in parallel. However, this is in practice not possible due to the limited FPGA resources that are available.

Revolutionary is the solution with the use of a fast space qualified FFT-coprocessor: the FFTC. The National Aerospace Laboratory (NLR) of the Netherlands has developed a Data Processing board, coined the On-board Payload Data Processing (OPDP), based on the FFTC ASIC that is developed under ESA license and available since early 2012. This chip, a rad-hard ASIC in the 0.18μ process of Atmel, can be regarded to be the fasted space qualified FFT-coprocessor in the world: it can perform FFT-operations of *1k* complex points in approximately 10 μs, with full floating point precision and it can perform up to *1M* points FFT in 20 ms, comparable with 5 GFLOPS operation speed.

Other typical applications for the OPDP are spectral imaging [10], interferometry [11] and 3D-altimetry, SAR data compression [12], SAR data processing and pulsar navigation for interplanetary missions [13].

OPDP MODULE

Modular setup

The OPDP board is equipped with the FFTC, glue logic and SDRAM memories. This Data Processing board gives the opportunity to process the GNSS signal faster than the current available space FPGAs or microprocessors. In 2009, NLR developed a prototype of the OPDP-concept, the E(Q)M-model will be ready at the end of 2013.

It consists of three boards and a backplane:

a) A LEON-board for general purpose processing and instrument control (based on GR712);
b) An FFTC-board for high-performance instrument data processing;

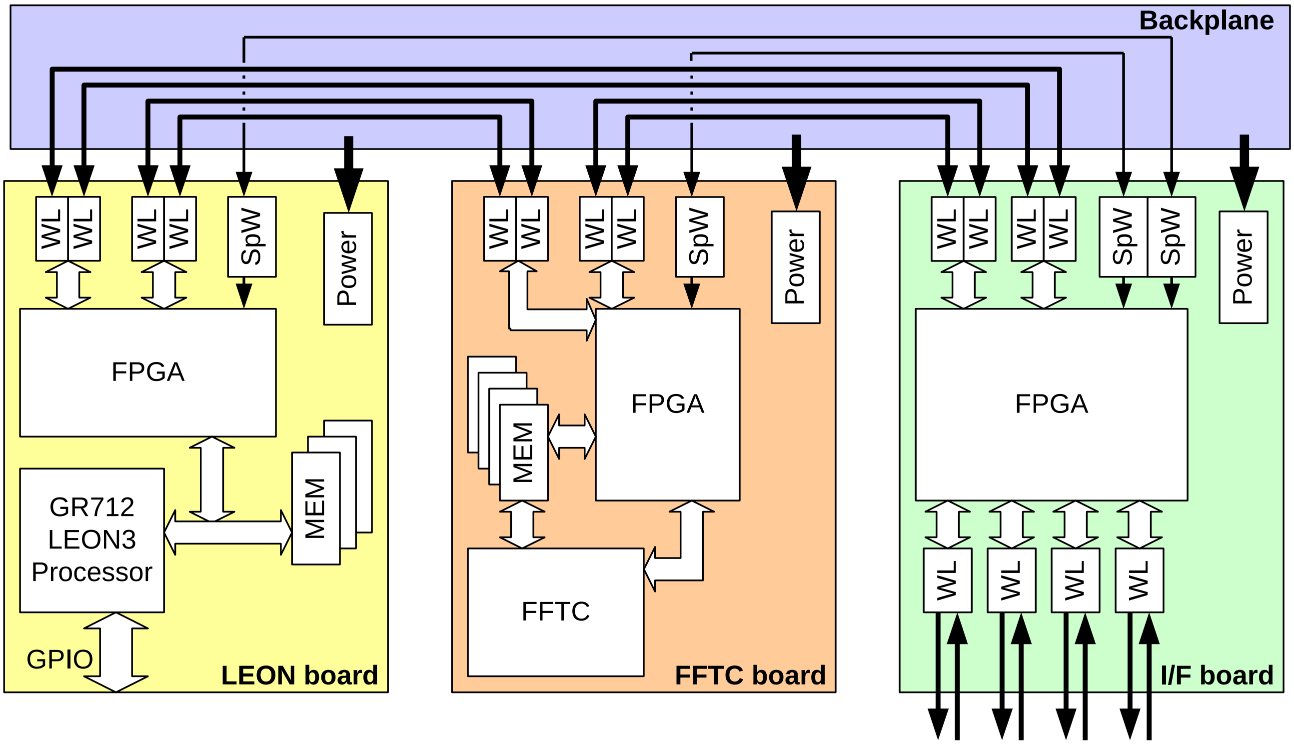

Fig. 3. OPDP schematic overview: LEON board, FFTC board and I/F board

c) An I/F-board with WizardLink I/O for high-speed interfacing and pre-processing of instrument data;
d) A passive backplane with high-speed data interconnect and power distribution.

The high speed data link of the I/F board is capable of transferring a data rate of up to 3.2 Gbits/sec (two parallel WizardLink interfaces). The interfaces on the backplane is designed such that the data throughput is not limited by the backplane. The choice for WizardLink (chipset: TLK2711) is based on the data rate that can be achieved, but also because in this way OPDP is *prepared* for extension to the SpaceFibre interface.
A schematic overview of the OPDP is shown in figure 3. The three boards (each single Eurocard size, 100 x 160 mm) give an extensive set of data processing capabilities, but with this modular setup and the open (backplane) interfaces of OPDP, the end customer gets many possibilities to adjust the OPDP concept to its own on-board data processing needs. As an example a number of different configurations are presented in figure 4.
For example, if the instrument requires a different interface (e.g. SpaceWire interfaces), the I/F-board can be replaced with a customized board. Another configuration is possible if the system engineer wants to combine the function of data processor and instrument controller. This can be done with OPDP by implementing an I/F-board with analogue and digital signals, controlled (if required) by the dual core LEON processor.
It is also possible that the system engineer prefers a different processor board, like the UT699 LEON3 processor, to optimize the usage of his simulation environment, re-use of pre-developed processor code or other heritage considerations.

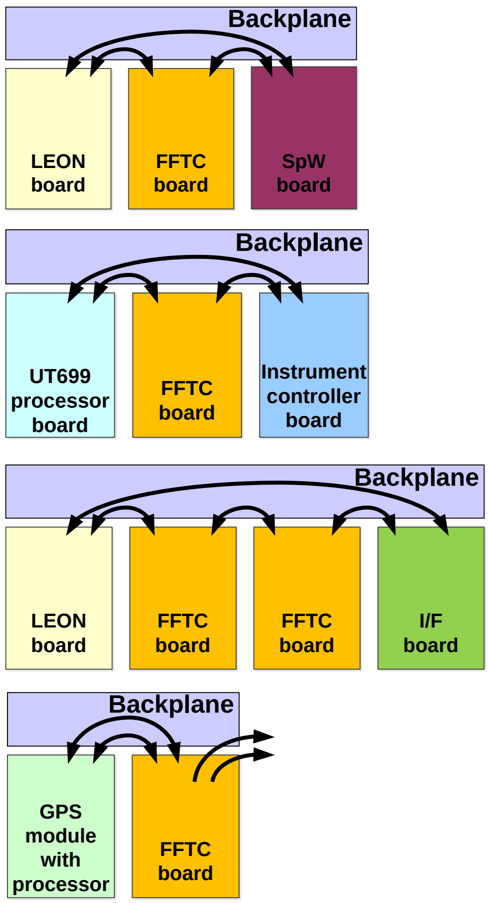

Fig. 4. Different configurations of OPDP

Table 1 OPDP Breadboard and E(Q)M

	Breadboard	**E(Q)M**
Processor board	LEON3 GR-CPCI-XC4V (Pender/Gaisler)	LEON3 Dual Core GR-712 (Gaisler)
FFT-chip	PowerFFT™ (Eonic BV)	FFTC (ESA/Atmel)
FPGA	ProAsic3000 (Actel)	RTAX-series (Actel)
SDRAM memory	K4S513233 (Samsung)	SD_4G64-series (3D-plus)
Assembly	Processor board FFTC-board	LEON-board FFTC-board I/F-board
Backplane	cPCI	Dedicated open interface on WizardLink (TLK2711)
Command & Control	Ethernet	SpaceWire
Data interfaces	Ethernet and SpaceWire	2x WizardLink (in) 2x WizardLink (out)

Also the implementation of special (or classified) data processing, which for example cannot be implemented in the FFTC, can be accommodated by usage of a dedicated data processing board in the third slot (e.g. with an FPGA). If fast 2D FFT-processing is required, two FFTC boards can be set in series for concatenated FFT-processing (one board for row, one board for column FFT processing).
The FFTC board can also be used in a standalone configuration, as long as it can obtain its algorithm and settings over a command interface (backplane) and its data over its incoming WizardLink interface. The result could be send over the FFTC outgoing WizardLink interface.
Table 1 summarizes the components of OPDM E(Q)M. The breadboard will be introduced in the testing section.
The FFTC is an ASIC consisting of an Arithmetic Logic Unit (ALU) block in combination with an FFT core. Functions of the ALU are add, subtract, multiply; functions of the FFT core are small FFT (*1k* points, in batch mode), inverse FFT, conjugate FFT, inverse conjugate. Next to the ALU and the FFT core, the FFTC is equipped with 4 memory ports for intermediate results.

The FFTC board is equipped with an FPGA to take care of the low level control of the FFTC, the appropriate addressing of the 4 memory ports of the FFTC and the queuing of the FFTC commands. The end user gets a set of high level commands to control the data stream and its operations on the FFTC. This includes corner turning (horizontal write, vertical read or vice versa) and data switching for continues data throughput.

Cooley Tukey method

The FFTC device is capable of performing FFT operations up to *1k* complex points. For longer FFT-operations (up to 1 million) the FFT can be calculated using the "Cooley Tukey" method explained in figure 5 [14]. The large data set is split in smaller subsets on which FFTs are calculated. After a multiplication with so-called twiddle factors a second FFT is calculated. This gives the same results as one FFT over the complete set: if a FFT is needed on a dataset of *N* samples, the data set is split into *N2* subsets with size *N1* (*N = N1 x N2*). This can be represented as a matrix of size *N1 x N2*. The Cooley Tukey method consists of four steps:

(1) the FFT is calculated row wise, on the *N1* subsets (*N2* times).
(2) The matrix is multiplied with *N1 x N2* twiddle factors.
(3) FFT is calculated colomn wise, on the *N2* data sets (*N1* times).
(4) The matrix is transposed for correct read-out.

The same method can be used for the inverse FFT operation or conjugate FFT.

TESTING OPDP FOR GNSS DATA PROCESSING

Test Setup

For testing purposes we have made use of a breadboard model of the OPDP. The breadboard (figure 6) is designed and assembled by NLR in 2010. It is based on commercial components but, from functional point of view, similar to the E(Q)M model of the OPDP. The breadboard consists of two boards: a processor board (LEON3 IP core on a commercial GR-CPCI-XC4V board) and a FFTC-board (with the commercial version of the FFTC, called PowerFFT™). Both boards are installed in a cPCI rack with a cPCI backplane interconnection. The data throughput over cPCI is not as fast as over the foreseen backplane of the E(Q)M but in both cases full transparent. For the external data interface(s) the breadboard uses the Ethernet connection of the processor board or a single SpaceWire interface.
We have tested the applicability of this Data Processing board, based on this FFTC co-processor, for GNSS applications with an acquisition algorithm utilizing GPS data collected with a software receiver.

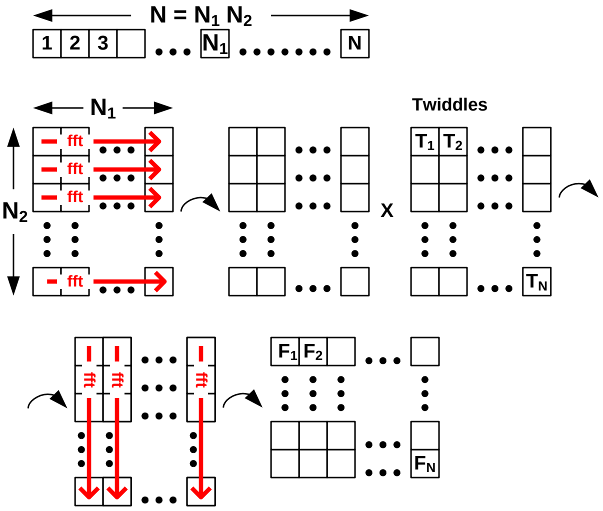

Fig. 5. Cooley Tukey method for large FFTs

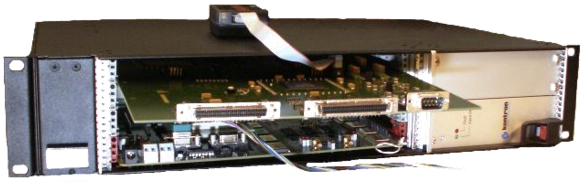

Fig. 6. OPDP breadboard with processor board (bottom) and FFTC board (top)

Approach

The model of a GNSS-R payload, based on the PARIS approach, is shown in figure 7: the direct signals, received at the zenith-pointing antenna, are combined directly with the reflected signals received at the nadir pointing antenna. The payload can be divided into two functions: navigation and GNSS-R.

The navigation functionality is the same as an ordinary GPS receiver; the GNSS-R is the remote sensing technique. In such a GNSS-R payload, the FFTC could be utilized for fast acquisition of the direct signals required for navigation, besides detecting the reflected signals.

For navigation, the signal acquisition has to be performed when the receiver is switched on -and if the user position is unknown- over a range of Doppler shifts and code phases for all GNSS satellites. For GNSS-R processing, normally the user position and GNSS satellite positions are available, and the reflection points of the visible GNSS satellite can be predicted, therefore the PRN code is known and the Doppler shift can be predicted, making the signal processing less demanding than the acquisition in cold start, which will be tested in this section.

The acquisition process makes use of the FFT, inverse FFT (IFFT) and complex conjugate of the FFT (FFT^*) mathematical operators to obtain the maximum of the following function:

$$\boldsymbol{R} = \boldsymbol{IFFT}(\boldsymbol{FFT}(\boldsymbol{D})\boldsymbol{FFT}^*(\boldsymbol{A})) \qquad \textbf{(1)}$$

where *D* is the direct signal down-converted to baseband, and *A* can be either a locally generated replica of the signal or the down-converted reflected signal.

In the algorithm all 32 satellite-IDs and *N* samples are, in the frequency domain, multiplied with a pre-defined data-set by performing a FFT operation. The result gives a peak value for the received sat-ID and the code-offset. In a small loop construction, the Doppler shift is determined, resulting in fast acquisition of the GPS signal.

In this example, we have *N* samples of the GNSS data. For applying the 'Cooley Tukey' method, this data set can be split up in *2N/1k* sets of *1k/2* samples and, with twiddle factors, the *N* (inverse) FFT can be calculated. The twiddle factors are stored in a memory port connected to the FFTC.

A detailed description of the individual steps is shown in Figures 8 – 10. In step 1 the complex conjugate of the FFT of a generated replica signal and the twiddle factors are loaded in the first and second memory respectively.

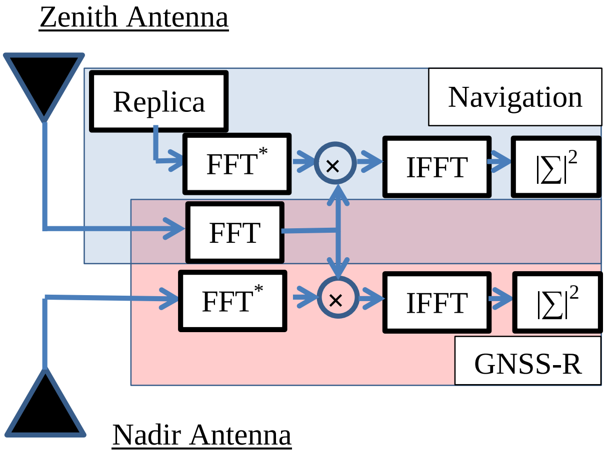

Fig. 7. GNSS-R Payload Design

If the replica signals are not stored in memory, they could be generated using a similar process as described by step 2 and 3.

In step 2, the down-converted GNSS data is loaded toward the input port of the FFTC and after performing FFTs on *1k* points stored into memory 4.

In step 3, with the so-called twiddle factors stored in memory 2, the complete FFT on *N* points is calculated and stored in memory 3.

In step 4 we multiply the outcome of the *N* FFT* of the replica signal and *N* FFT of GNSS data, perform IFFTs on sets of *1k* points and store the outcome in memory 4.

With use of the twiddle factors –still available in memory 2- the complete IFFT on *N* points is calculated and stored in memory 3.

In the last step the data in memory 3 could be send to the processor and/or to the I/F board.

Results

The required calculation time for acquiring the GNSS signals is estimated below. As mentioned earlier, the FFTC can perform a *1k* FFT in approx. 10 µs. and combine the multiplication with FFT operation in one step. In this example we utilize 38 MHz as sampling frequency and search for all 32 GPS satellite (32 PRNs) using 20 steps for Doppler search:

With *N* = 38*k* for 1 PRN:

Step2	*1k* FFT, 32 times	=	320 µs
Step3	32 point FFT, *1k* times (incl twiddle)	=	320 µs
Step4	Multiply result with replica, 1*k* IFFT, 32 times	=	320 µs
Step5	32 point IFFT, 1*k* times (incl twiddle)	=	320 µs
Total		=	1280 µs
		≈	1.3 ms

The time of each individual step is verified on the breadboard OPDP.

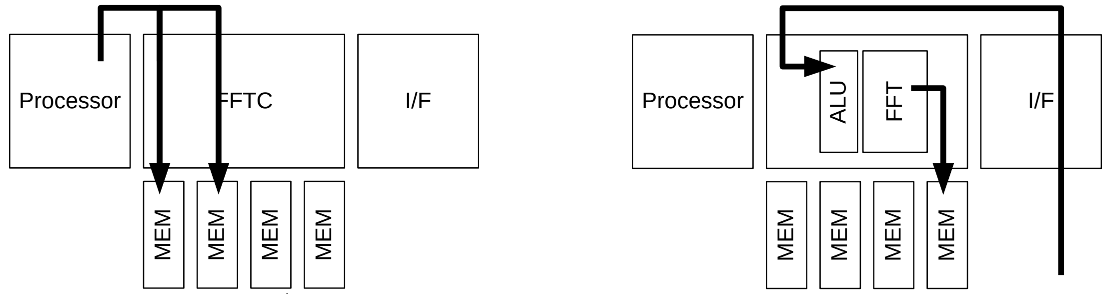

Fig. 8. Step 1 (loading FFT of replica and twiddle factors) and step 2 (perform 1k FFTs on raw GNSS data)*

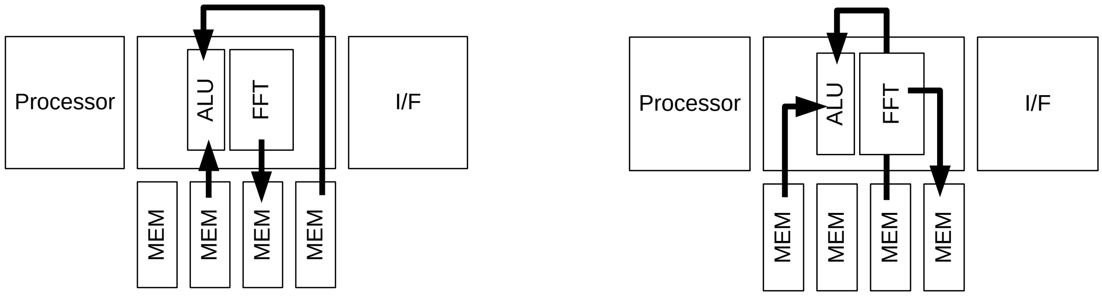

Fig. 9. Step 3 (use twiddle factors to perform FFT on N points) and step 4 (multiply FFT of replica and FFT of GNSS data and perform IFFTs on sets of 1k points)*

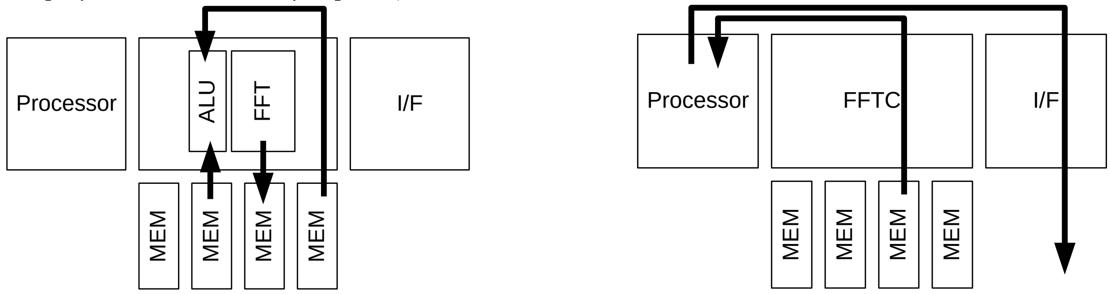

Fig. 10. Step 5 (use twiddle factors to perform IFFT on N points) and step 6 (output result)

These steps are performed for 32 PRNs, thus the total computational time is about 41 ms. With 20 steps for Doppler search, the signal acquisition without any prior knowledge could be performed within 1s computational time.

For reflected GNSS signals from selected GPS satellites with predicted Doppler, this type of calculations could be performed in real time.

Figure 11 shows the acquisition result - the normalized correlation amplitude - for the 2D search as a function of Doppler and code phase. For a certain Doppler and code phase combination -using the PRN code of satellite 21- a peak is detected. A detection threshold must be selected above which signal presence is declared.

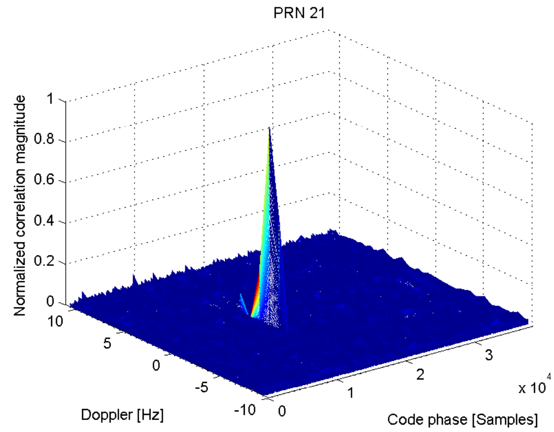

Fig. 11.Signal acquisition result for PRN 21

SUMMARY
GNSS reflectometry (GNSS-R) could become a powerful remote sensing technique for earth observation satellites. Demonstrations missions of this type of technology are currently under development. Fast processing power is desirable to process the GNSS data in real-time, avoiding the storage of large amounts of data on the satellite and downloading this data to the ground segment. The FFT has been demonstrated to be a computational efficient approach for GNSS signal processing.
This paper presented a detailed description of a space qualified FFT-Coprocessor unit and it's potential for spaceborne GNSS applications including GNSS-R. Moreover, the co-processor could be utilized for fast GNSS signal acquisition after power on of a GNSS receiver and for reacquisition of the GNSS signals after a latch-up which could occur due to radiation in the space environment.

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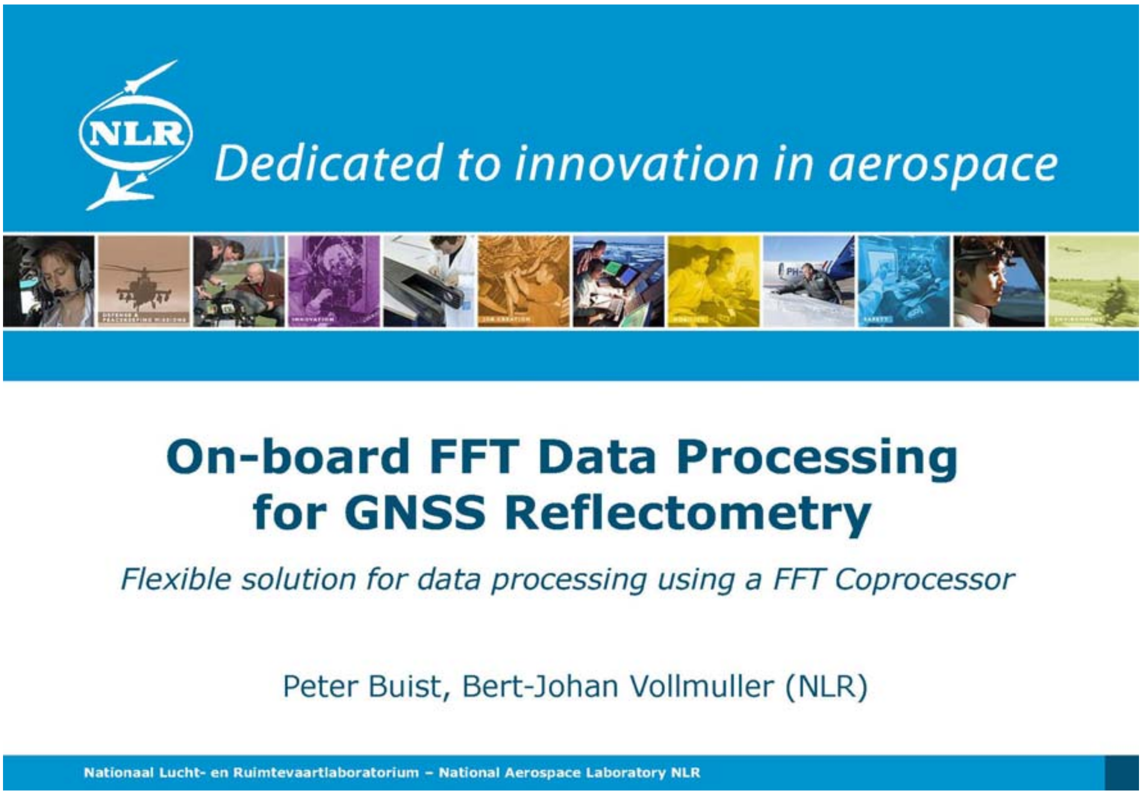
Appendix A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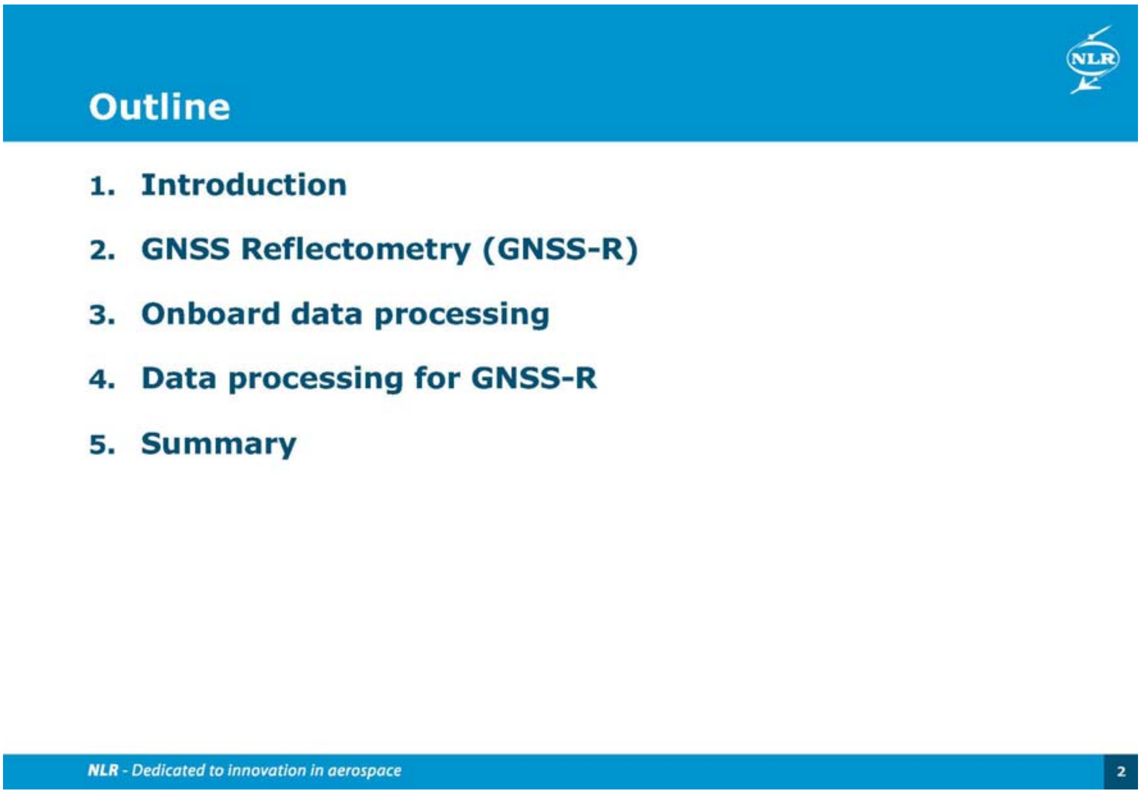
On-board FFT Data Processing
for GNSS Reflectometry
Flexible solution for data processing using a FFT Coprocessor
Peter Buist, Bert-Johan Vollmuller (NLR)
Nationaal Lucht- en Ruimtevaartlaboratorium – National Aerospace Laboratory NLR


Outline
NLR
1. Introduction
2. GNSS Reflectometry (GNSS-R)
3. Onboard data processing
4. Data processing for GNSS-R
5. Summary
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Outline

1. Introduction
2. GNSS Reflectometry (GNSS-R)
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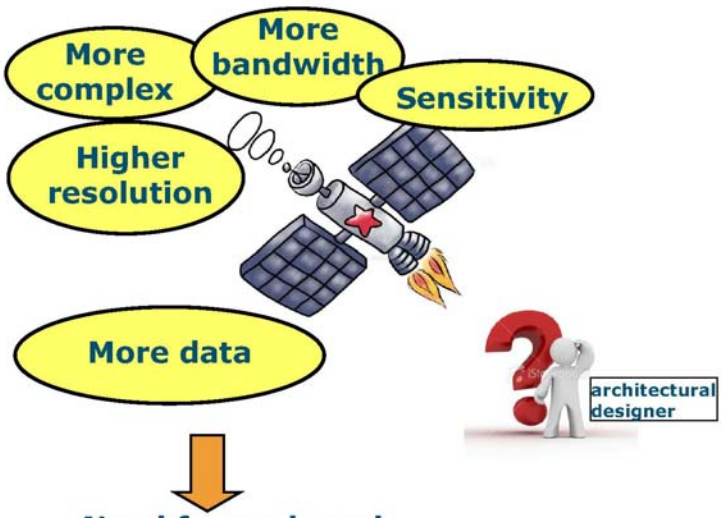
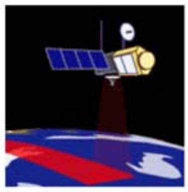
1.1 Introduction



Need for on-board computational power

1.2 Introduction

- The flexible solution for any satellite that requires FFT
  - SAR satellites (processing - compression)
  - 3D-Altimeter
  - Spectral Imaging (Multi-, hyperspectrum)
  - Interferometry
  - Pulsar navigation
  - Etc.



- All FFT-operations (Single FFT, 2D-FFT etc)
- Flexibility of Leon-processor
- Flexibility of algorithm
- Modularity ➔ flexible in interfacing

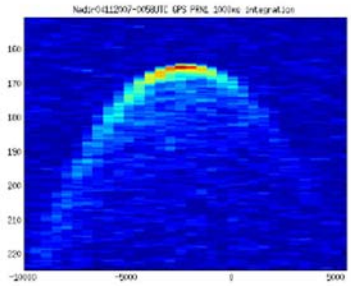
- Data processing / data compression at high data rate

Outline

1. Introduction
2. GNSS Reflectometry (GNSS-R)
3. Onboard data processing
4. Data processing for GNSS-R
5. Summary

2.1 GNSS Reflectometry

- **GNSS reflectometry (GNSS-R) introduced by Martin-Neira in 1993**
- **Powerful remote sensing technique**
  - ocean altimetry (Delay), sea state (Distortion), etc.
- **Some 150 GNSS satellites to be available in the near future**
- **Fast processing power to process in real-time, avoiding the storage of large amounts of data and downloading to the ground segment**



Delay Doppler Map (©SSTL)

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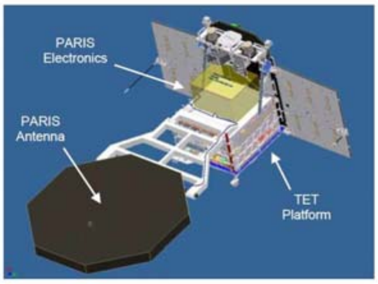
2.2 GNSS-R missions



PARIS payload on TET platform (©ESA)

Satellite of the CYGNSS constellation (©University of Michigan)

- **Space qualified microprocessor -> not very fast**
- **Faster with an implementation in VHDL in a space qualified FPGA**
  - **In practice not possible due to limited resources**

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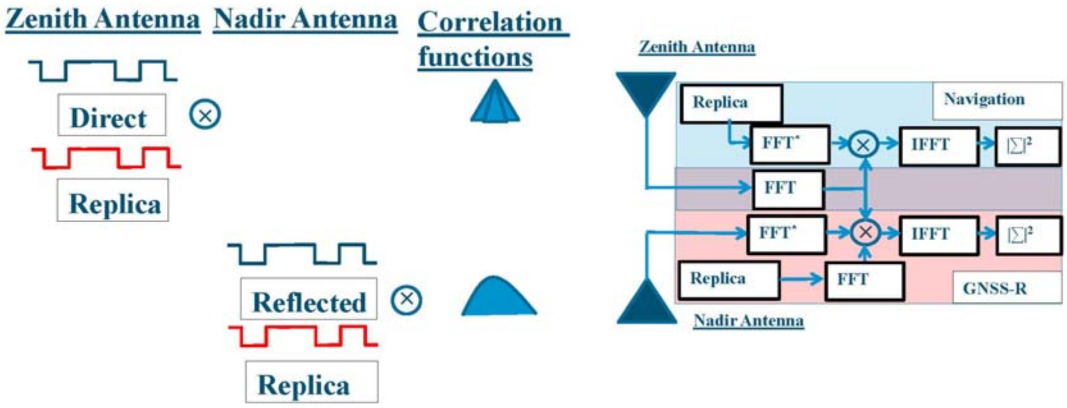
2.3 GNSS-Reflectometry



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3.1 OPDP (On-board Data Processing)

- **OPDP = Leon3 + FFTC**
- **Benefits of OPDP:**
  - FFTC options:
    -- single 1024-points FFT in 10μs
    -- up to 1Msamples FFT
    -- many data formats
    -- FFT, FFT^{-1}, Conjugate, Multiplication, Extraction, etc.
    -- Arithmetic Logic Unit (ALU) - add, subtract, multiply
    -- fasted space qualified FFT-coprocessor in the world
  - Flexibility of the Leon-processor
  - Flexibility of 'algorithm'
  - Flexibility of modular design
  - Sustained data throughput of 95 Mcps

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3.2 Fast Fourier Transform Coprocessor

- **ESA obtained PowerFFT license from Eonic (Delft, Netherlands)**
- **ESA contract to Astrium/Actel to 'space qualify' PowerFFT into FFTC**

- **ASIC build in the MultiWaferProject of ESA**
- **0.18u RHA process of Atmel**
- **In 2001 selected by ESA for space qualification**
  - Large set of functions
  - Floating point accuracy
  - High processing speed (100 MHz / 64 bits complex /5 GFLOPS)
- **Samples available since 2012**

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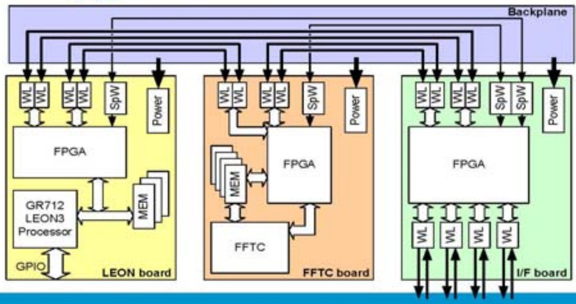
3.3 OPDP Design

- Three boards (single Eurocard size, 100 x 160 mm)
- Modular setup
- Open (backplane) interfaces of OPDP
- Adjust the concept to on-board data processing needs
- 2009, prototype; 2013 the E(Q)M-model



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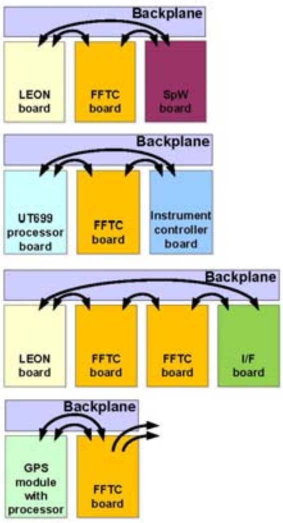
3.4 Configurations

- A different interface
- Different processor board
- Fast 2D FFT-processing -> two FFTC boards can be set in series for concatenated FFT-processin
- Standalone configuration



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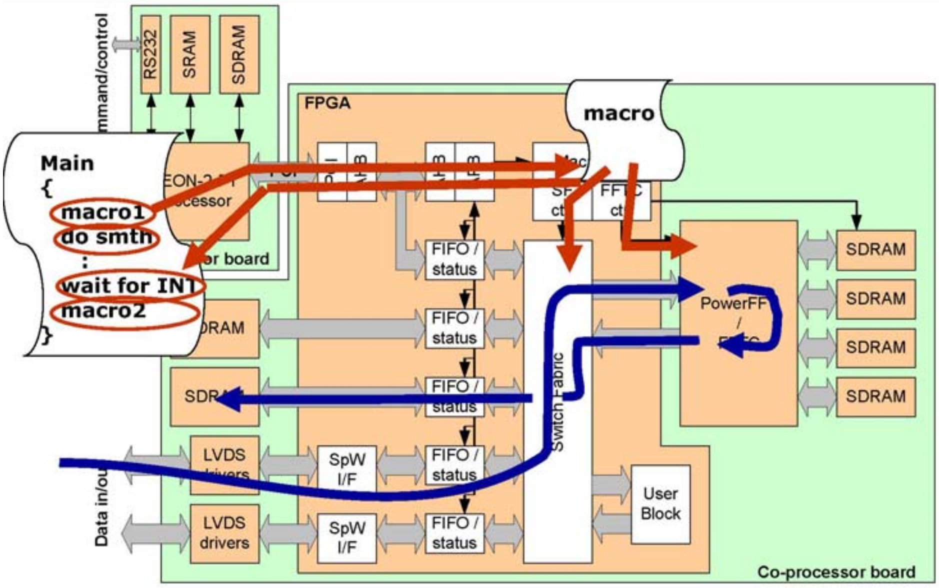
3.5 On-board Data Processing



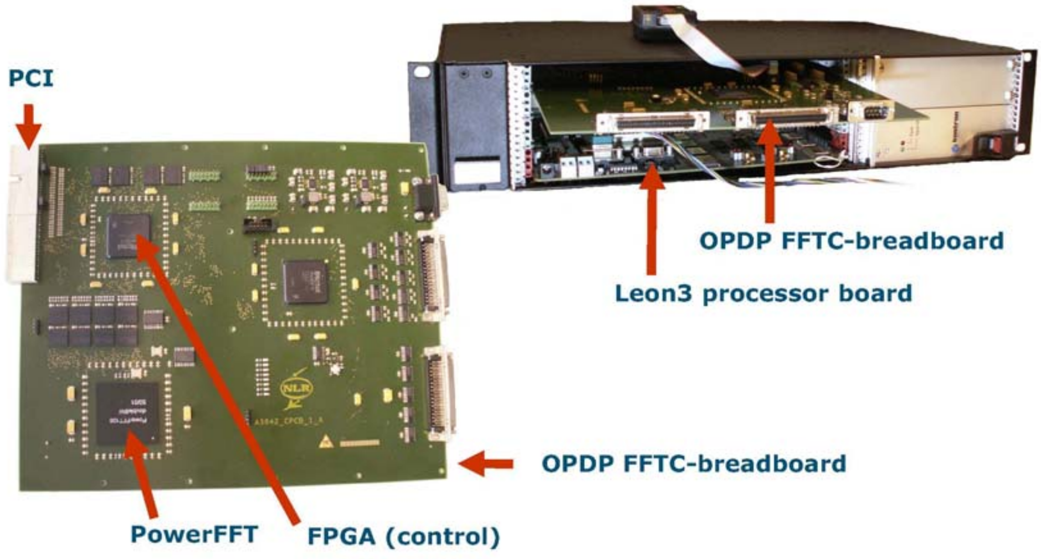
3.6 Breadboard and E(Q)M

	Breadboard	E(Q)M
Processor	LEON3 GR-CPCI-XC4V (Pender/Gaisler)	LEON3 Dual Core GR-712 (Gaisler)
FFT-chip	PowerFFT™ (Eonic)	FFTC (ESA/Atmel)
FPGA	ProAsic3000 (Actel)	RTAX-series (Actel)
SDRAM memory	K4S513233 (Samsung)	SD_4G64-series (3D-plus)
Assembly	Processor board FFTC board	LEON-board FFTC-board I/F-board
Command & Control	Ethernet	SpaceWire
Data interfaces	Ethernet and SpaceWire	2x WizardLink (in) 2x WizardLink (out)

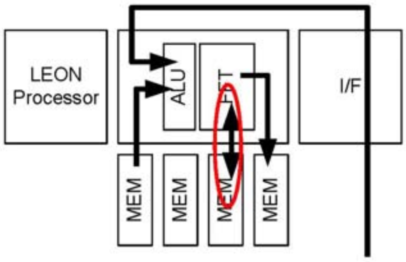
Outline

1. **Introduction**
2. **GNSS Reflectometry (GNSS-R)**
3. **Onboard data processing**
4. **Data processing for GNSS-R**
5. **Summary**

4.1 Breadboard



4.2 Cooley Tukey method



The FFTC-control
→ corner turning
→ Cooley Tukey
→ long FFT (upto 1 million points)

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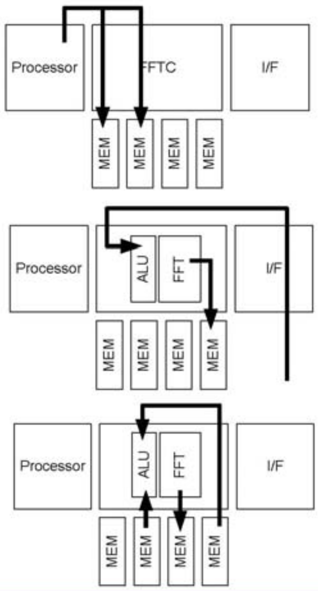
4.3 Data Processing:

- **Acquisition algorithm**
- **GPS data collected with a software receiver**
- **Testing with breadboard model**
- **Commercial components**
  - processor board (LEON3 IP core on GR-CPCI-XC4V board)
  - FFTC-board (PowerFFT™)
- ***Maximum of***
  $R = IFFT(FFT(D)FFT^{*}(A))$



step1: loading FFT* of replica and twiddle factors

step2: perform 1k FFTs on raw GNSS data

step3: use twiddle factors to perform FFT on N points

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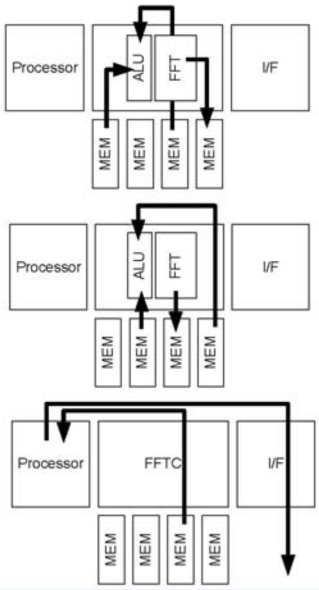
4.4 Data Processing:



step4: multiply FFT* of replica and FFT of GNSS data and perform IFFTs on sets of 1k points

step5: use twiddle factors to perform IFFT on N points

step6: output result

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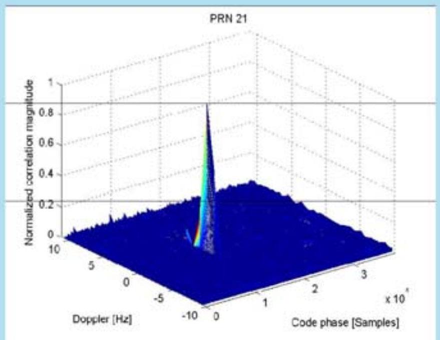
4.5 Test with breadboard model and data from software GPS receiver

With *N* = 32*k* for 1 PRN:

- **Step2 *1k* FFT, 32 times = 320 μs**
- **Step3 32 point FFT, *1k* times = 320 μs**
- **Step4 Multiply with replica, 1*k* IFFT, 32 times, = 320 μs**
- **Step5 32 point IFFT, 1*k* times = 320 μs**



- **Total = 1280 μs ≈ 1.3 ms**
- **1.3 x 32 PRNs x 20 Doppler steps ≈ 1 s**

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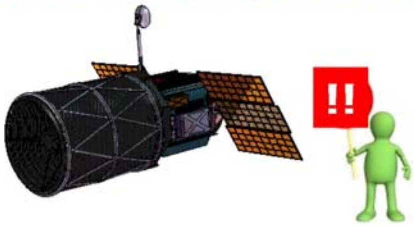
5.1 Summary GNSS-R

- GNSS reflectometry is a powerful remote sensing technique
- Demonstration missions are under development
- Fast processing power is desirable to
  - process the GNSS data in real-time
  - avoiding the storage of large amounts of data and downloading to the ground segment
- The FFT is a computational efficient approach for GNSS signal processing

5.2 Summary OPDP

- **OPDP is space qualified data processing unit with FFT-capabilities**
- **Potential for GNSS-R**
- **OPDP board is**
  - High speed data processing – flexible/programmable
  - Due to combination of LEON and FFTC
  - Customer configurations
  - FFT-processing without the need for designing the FFTC control from scratch



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ACKNOWLEDGMENTS

- **Current OPDP development is performed under a contract with ESA/ESTEC (TEC-EDP), under the responsibility of Dirk Thurnes and Martin Suess**
- **The breadboard model was developed with support of the Netherlands Space Office.**

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