Nationaal Lucht- en Ruimtevaartlaboratorium
National Aerospace Laboratory NLR

NLR TP 97360

Mass storage device developed for application in the space station

T. Algra

DOCUMENT CONTROL SHEET

	ORIGINATOR'S REF. NLR TP 97360 U		SECURITY CLASS. Unclassified

ORIGINATOR
National Aerospace Laboratory NLR, Amsterdam, The Netherlands

TITLE
Mass storage device developed for application in the space station

PRESENTED AT
the 48th International Astronautical Congress, October 6-10, 1997, Turin.

AUTHORS T. Algra	DATE 970722	pp 11	ref 2

DESCRIPTORS
Computer storage devices
Data storage
Data acquisition
Environmental tests
Latch-up
Magnetic disks
Memory (computers)
Protocol (computers)
Radiation protection
Real time operation

ABSTRACT
Data storage devices each providing 260 MB non-volatile random access memory will be used in the Data Management Systems of the Russian and the European Modules of the Space Station. The National Aerospace Laboratory NLR, and Signaal Special Products have jointly developed these Mass Storage Devices (MSD) based on commercial winchester disks. For increased reliability, these MSDs contain two separate disk cartridges with identical data contents. An intelligent latch-up protection system has been incorporated to safeguard the drives against destruction due to radiation effects. This protection mechanism has been validated by tests in a proton beam facility.

MASS STORAGE DEVICE DEVELOPED FOR APPLICATION IN THE SPACE STATION

T. Algra
National Aerospace Laboratory NLR
P.O.Box 153, 8300 AD, Emmeloord, The Netherlands
E-mail: algra@nlr.nl

ABSTRACT

Data storage devices each providing 260 MB non-volatile random access memory will be used in the Data Management Systems of the Russian and the European Modules of the Space Station. The National Aerospace Laboratory NLR, and Signaal Special Products have jointly developed these Mass Storage Devices (MSD) based on commercial winchester disks. For increased reliability, these MSDs contain two separate disk cartridges with identical data contents. An intelligent latch-up protection system has been incorporated to safeguard the drives against destruction due to radiation effects. This protection mechanism has been validated by tests in a proton beam facility.

1 INTRODUCTION

The Russian Service Module of the International Space Station will be equipped with a Data Management System (DMS-R) to be built by a European industrial consortium under ESA responsibility. The DMS-R includes two so-called Control Post Computers. These computers, developed under responsibility of Matra Marconi Space France, are driven by a SPARC processor configuration, based on VME architecture (10 slots), and equipped with MIL-STD-1553B and Ethernet interfaces. The Control Post Computers each contain a Mass Storage Device (MSD)

Based on non-volatile memory technology, these units will provide storage capacity for DMS system software and payload data.
As much as possible, the elements of the DMS-R will be re-used for the realisation of the DMS of the European module of the Space Station, the Columbus Orbital Facility (COF). For example, the MSD will be a part of the MMU (Mass Memory Unit) computer.

Signaal Special Products (SSP) together with the National Aerospace Laboratory (NLR), both of the Netherlands, developed and used a design and implementation approach for the MSD, which is relatively cost-effective by employing Commercial-Of-The-Shelf winchester disk drives. The selected drives are PCMCIA type 3 drives with a storage capacity of 260 MB. The small dimensions (86 x 54 x 10.5 mm) allow the disk drives to be accommodated in removable cartridges. These cartridges are hermetically sealed for two reasons: i) the drives require at least 0.6 Bar environmental pressure during operation, ii) the drives contain components and materials that are not manufactured according military or space quality standards.
In order to meet the applicable vibration and shock requirements, the drives are protected by a suspension system inside the cartridges. The selected drive meets the other basic environmental requirements except the radiation susceptibility (see Section 3). Temperature screening of the drives has been included in the MSD manufacturing cycle for the qualification with respect to temperature extremes.
The cartridges are removable and exchangeable. The standardized PCMCIA interface offers a number of advantages:
- growth potential: the disks can be easily replaced by future higher-density types without the necessity to redesign the MSD;

- existing hardware and software components can be used in ground support and test equipment;
- the fully documented and supported PCMCIA interface reduces efforts required for controller development;
- the design of the MSD may be used in the future for other Commercial-Of-The-Shelf PCMCIA applications such as Ethernet cards, video interfacing and compression, and A/D conversion, without the need for hardware modifications.

Fig. 1 gives an impression of the complete unit. Fig. 2 depicts a block diagram of the system. The MSD contains two cartridges with a disk drive, with identical data contents. This allows mirror mode operation to improve system reliability. A controller board has been developed with the following basic functionality: VME to PCMCIA interfacing, mirror mode operation, and latch-up protection. The MSD occupies three slots in the VME crate of the Control Post Computer. The disks can be formatted (DOS 5) and preloaded with software and/or data, using a Ground Support Tool, basically a PC equipped with a PCMCIA interface extended with a "flight" connector compatible to the cartridge. The MSD has been designed for 10 years operational lifetime.

2 MSD CONTROLLER

The controller interfaces the VME bus to the two drives (Fig. 3). It supports the VME protocol at one side and the PCMCIA ATA protocol at the other side to transfer data between a host processor and the drives.
In addition, the controller provides the following functions:
- data duplication and verification in the mirror mode;
- generation of status information;
- monitoring of the power supply currents of the drives and protection of the drives against circuit burnout due to radiation effects (refer to Section 3).

The controller supports two operational modes: mirror mode and single mode. In the mirror mode the data written to drive 1 are automatically and simultaneously written to drive 2 as well. When reading data, the controller accesses and reads both drives and compares the two data streams on the fly. In case of a difference, the controller signals the host by an interrupt. Differences may occur due to radiation effects or a drive defect. The probability of bit errors caused by radiation in orbit is extremely low. Nevertheless, these errors can be corrected for by the host. The mirror mode is the default operational mode, providing increased system reliability. A special feature in this mode is the verify command, providing the option to compare the data contents of the two drives by the controller, without data transfer over the VME bus.
In the single mode, data is transferred between the host and one drive (selected by command).
The controller electronics at the VME bus side is defined as a VME Slave Module supporting byte and word transfers (including block transfer). All the control and I/O registers of the drives are mapped to VME memory and are directly accessible for the host processor. A command register and a status register are included on the controller board to direct and to monitor the drive command and transfer processes. By the command register the following command options are available to the host: reset, initiate verify function, mask interrupt, enable latch-up detection, and select mode (single or mirror). The status register gives information on the power-on status of the drives, pending interrupt requests, microcontroller health, and verify status. The host is interrupted upon any change of the controller's status register.
The PCMCIA interfaces to the two drives are completely separated, to prevent any fault propagation from one drive to the other. For both drives an electronic short circuit protection function has been included.
The controller electronics are assembled on a printed circuit board (PCB) which is mounted inside the unit. This PCB is provided with a conduction cooling plate with a heat management layer. The PCB assembly is mounted between the unit's top and bottom

frames which are in close thermal contact to the cooling plate. The unit is positioned in the VME rack and clamped by expanders to assure mechanical rigidity and thermal contact between the unit and the rack.

3 LATCH-UP PROTECTION FUNCTION

The disk drives contain microcircuits which are sensitive to radiation effects, in particular so-called Single Event Upsets. The basic mechanism of Single Event Upset is the deposition of charge by the passage of a heavy ion through the sensitive region of a device. If the ion has enough stopping power the charge may be sufficient to change the state of an electrical node or cell within a device. The best known example of this is the change in state of a memory cell which can be subsequently rewritten. This is known as a soft error which may be defined as an erroneous but correctable logic state. A more dangerous form of upset is heavy ion induced latch-up[1]. In a CMOS device a deposited charge may cause a low-impedance path. This state is permanent as long as the device remains powered, and results in a potentially destructive high current through the device. A latch-up state can be removed by powering off the device for a while immediately after the occurrence of the event. This prevents damage to the microcircuit.

To detect instantaneous rises due to latch-up events, the supply currents of the two drives are continuously monitored . The architecture of the latch-up protection function is included in Fig. 3. Power is supplied to the drives through an electronic switch and a current sense resistor. The currents are measured, digitized, and read by a microprocessor. This processor compares the currents with an adaptive threshold. Using a specially designed algorithm, noise and other variations are excluded and a reliable latch-up detection is realized. As soon as such a latch-up is detected, the microprocessor drives the electronic switch in the off state long enough to remove the latch-up condition. The microprocessor simultaneously activates a bleeder circuit which rapidly removes internal charges. In addition, the event is reported to the host by an interrupt and status information. Note that the other drive is not influenced by this recovery process.

The bleeder circuit can also be activated directly via the VME bus, e.g. by the host processor. This feature is useful to test the latch-up protection function since the bleeder current can be regarded as a simulated latch-up current.

The supply current profile depends on the state of the disk and the command history. Therefore, the microprocessor algorithm continuously adapts the detection thresholds to the current situation. Variations due to temperature, measuring offset, and dispersion are also covered. Fig. 4 depicts a simplified state transition diagram of the microcontroller software (shown for one drive only).

4 DEVELOPMENT AND VERIFICATION

The development and verification programme included the realization of two Development Models (functionally equivalent to the end product), two Engineering Models (electrically equivalent), and a Qualification Model. The Qualification Model is equivalent to the flight models, including components, materials, and manufacturing processes applied. However, due to the tight project planning, the integration of the engineering model of the control post computer was still in progress during the production of the MSD Qualification Model. This approach was intended, and resulted in a number of modifications carried out on the MSD Qualification Model before the start of the qualification test programme. This model was intentionally referred to as "Engineering Qualification Model". It was also subjected to an extensive pre-qualification programme, mainly to verify procedures and design solutions with respect to the cartridge suspension system, the cartridge hermeticity, and temperature control issues.

A computerized Unit Tester (Fig. 5) has been developed for the functional and performance tests. The Unit Tester comprises two VME racks (host rack and rigid rack) and a PC. The host rack accommodates a power supply, a VME master/controller board, a custom test hardware board, and a VME extension board. The rigid VME rack, used as a fixture during the operational environmental tests, contains another, ruggedized VME extension board and the MSD under test. The two racks act like one VME rack by the use of extension boards. The Unit Tester software runs under a real-time operating kernel. The lowest level of the Unit Tester software comprises the MSD driver. The next level consists of modular test functions (read or write a block of data, put a drive in sleep mode, etc). At the highest level, automated test sequences are available, that execute predetermined sets of MSD test actions. These test sequences, written in a dedicated test language, are processed by an interpreter.

The latch-up protection function has been validated by proton irradiation at the Paul Scherrer Institute, Switzerland. For this validation a test set-up has been realized being a modified version of the MSD/Unit Tester configuration with provisions for extended PCMCIA cabling, data acquisition, and test software[2].

5 CONCLUSIONS

A Mass Storage Device with Commercial-Of-The-Shelf winchester drives has been developed. It is a non-volatile memory unit providing 260 MB random access memory in a VME environment, and has been designed for an operational lifetime of 10 years for application in the International Space Station. Compliance to all the applicable requirements has been achieved by a special cartridge accommodation method and an intelligent latch-up protection system. The adoption of the PCMCIA standard offers growth potential towards higher-density drives and opportunities for technology insertion.

6 REFERENCES

[1] Adams, L., "Cosmic ray effects in microelectronics", Microelectronics Journal, Vol. 16, No. 2, 1985

[2] Dorp, A.L.C. van, "Mass Storage Device Radiation Test Final Report", MSD-NLR-TN-031, issue 1, NLR, 1996

Table 1 Mass Storage Device specifications

ENVIRONMENT		
Vibration Random (20-2000 Hz)	Operating Non-operating	4.8 grms 21 grms
Shock	5 ms	40 g
Temperature	Operating Non-operating	0 - +40 °C -50 - +50 °C
Pressure		5 - 970 mm Hg
Radiation	SEU	SEL protected
PERFORMANCE		
Interfaces	VME Disks	IEC 821 / IEEE 1101.2 PCMCIA ATA
Data capacity		2 x 260 MB
Power	DC input voltages +5 V current	+ 5 V ± 2.5% +12 V; -12V 2.1 A peak
System performance	Read transfer rate Write transfer rate Max. access time	780 kByte/s 955 kByte/s 18 ms
Physical	Size Weight	3 VME slots 2650 g
Reliability	BER MTBF (30 °C)	$< 10^{-14}$ 9E5 hrs

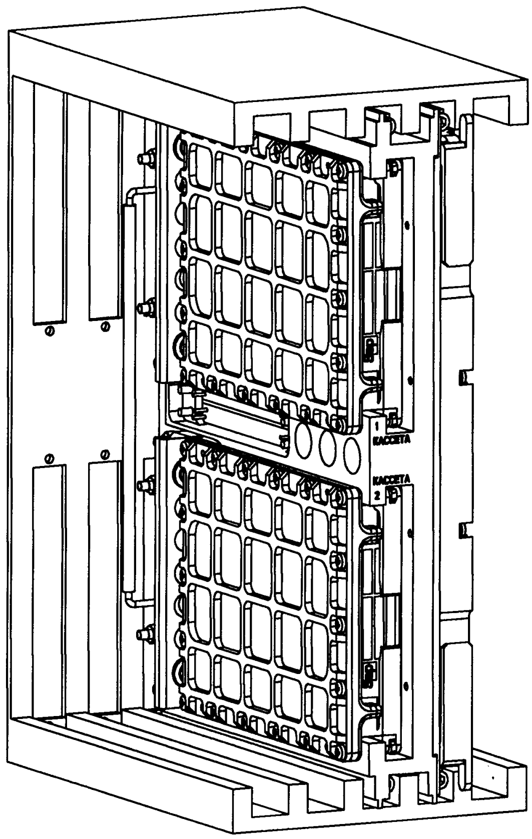

Fig. 1 Mass Storage Device

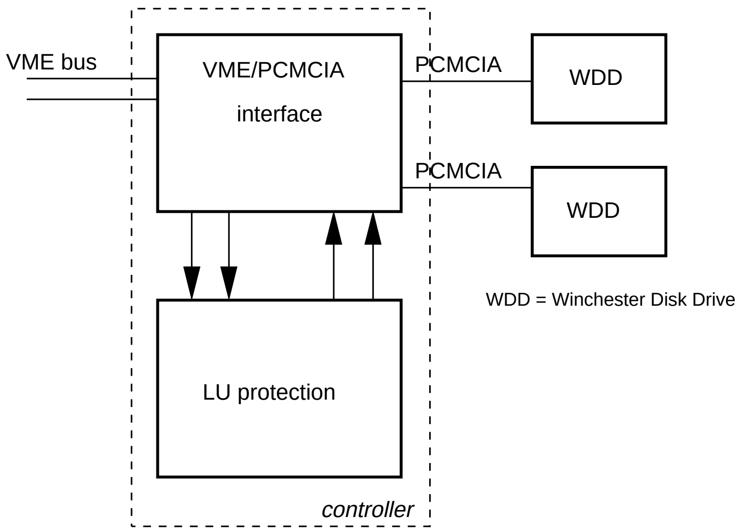

Fig. 2 MSD block diagram

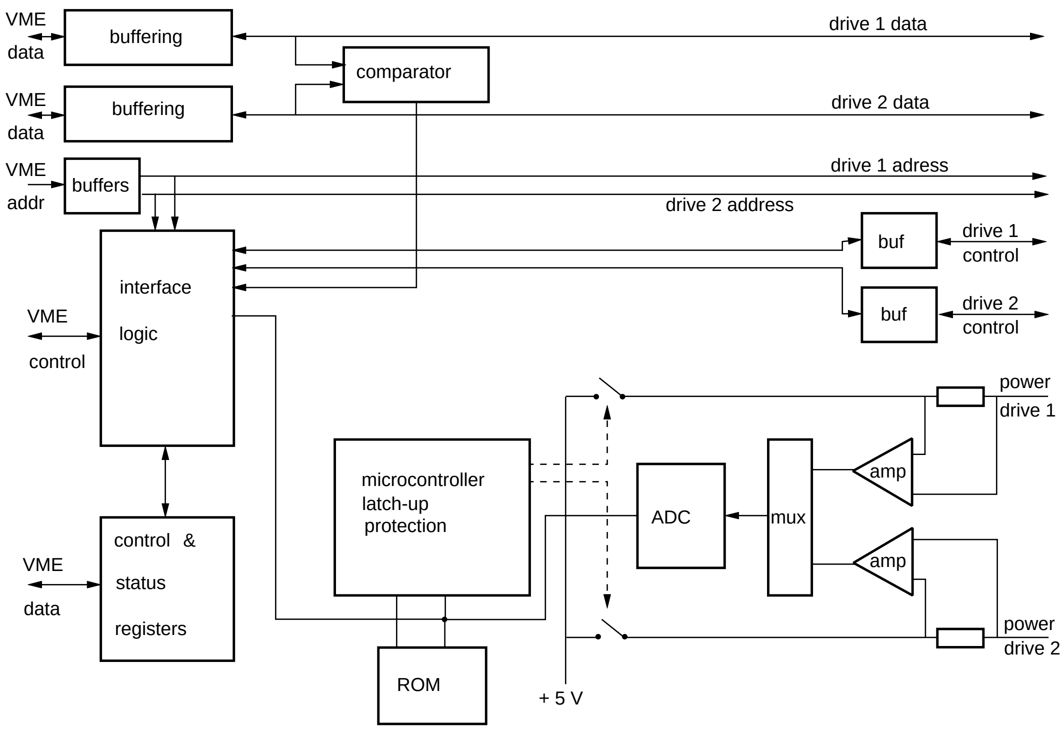

Fig. 3 Architecture of MSD controller

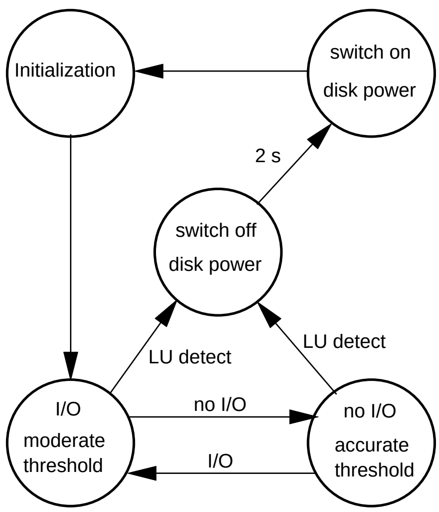

Fig. 4 Simplified state transition diagram of latch-up protection software

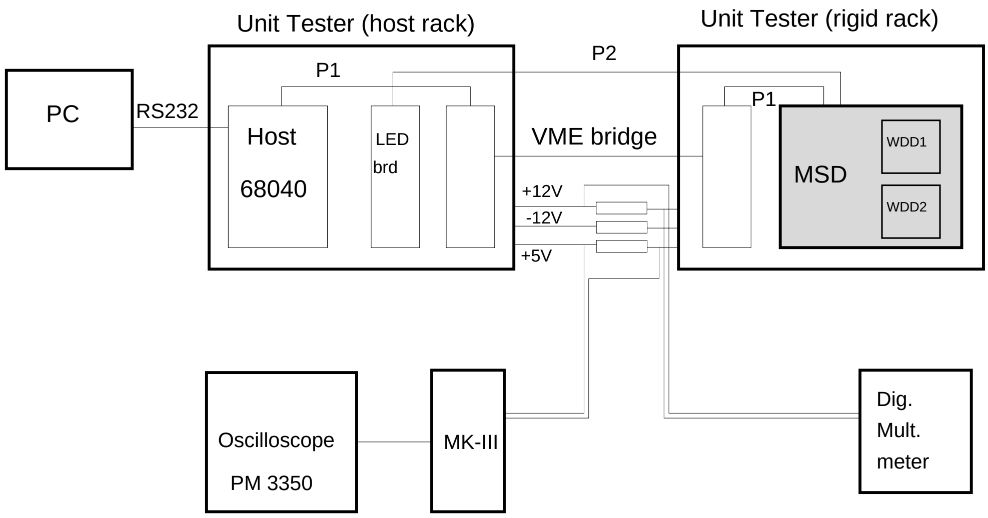

Fig. 5 MSD Unit Tester