Nationaal Lucht- en Ruimtevaartlaboratorium
National Aerospace Laboratory NLR

Executive summary

On-board Payload Data Processing module

Problem area
The increasingly demanding signal and image processing requirements for on-board payloads comes from issues such as the need for more bandwidth, higher sensor resolutions and sensitivities, better data compression, more accurate and adaptive calibration techniques, spacecraft autonomy and more. The current generation of space-qualified Digital Signal Processors (DSP), however, does not meet the requirements of advanced missions anymore. ESA recently initiated the development of a next generation DSP device, but it will probably take up to a decade before such a component can be brought into production. Therefore, for the shorter timeframe, an alternative must become available.

Description of work
This paper describes the architecture of an "On-board Payload Data Processing" (OPDP) board. This generic processor board is highly flexible, and due to its modular design, it will fit in different payload data handling systems for a wide range of missions. It is extremely powerful for on-board image and signal processing through the combination of the general purpose AT697 LEON processor and the flexible FFT-oriented DSP co-processor FFTC (Fast Fourier Transform Co-processor).

Results and conclusions
The presented On-board Payload Data Processing module architecture can be used in a broad range of mission applications. It is a reconfigurable and reprogrammable module with a high data throughput speed, based on a space-qualified general purpose processor, and the FFTC, a space-qualified FFT-oriented DSP co-processor. The OPDP supports an extensive set of existing and future interfaces such as SpaceWire, SpaceFiber, MIL-1553, CAN, and other high-speed data links, and is compatible with ESA-advocated payload data handling architectures.

Applicability
Such an OPDP board allows the implementation of advanced payload data processing functions on board of satellites. For example any altimeter mission can benefit from these fast FFT-oriented processing capabilities to improve its resolution. Other potential applications are filtering, SAR processing, compression, spectrometry functions and more.

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On-board Payload Data Processing module

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Contents

ON-BOARD PAYLOAD DATA PROCESSING MODULE

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ABSTRACT

Remote sensing payloads in satellite missions are becoming increasingly complex, resulting in more demanding requirements for on-board processing. Standardization en re-use of technologies are also of essential importance for the efficient development, implementation and use of space systems. This paper describes the architecture of an "On-board Payload Data Processing" (OPDP) board. This generic processor board is highly flexible, and due to its modular design, it will fit in different payload data handling systems for a wide range of missions. It is extremely powerful for on-board image and signal processing through the combination of the general purpose AT697 LEON processor and the flexible FFT-oriented DSP co-processor FFTC (Fast Fourier Transform Co-processor). Such an OPDP board allows the implementation of advanced payload data processing functions on board of satellites. For example any altimeter mission can benefit from these fast FFT-oriented processing capabilities to improve its resolution. Other potential applications are filtering, SAR processing, compression, spectrometry functions and more.

1 INTRODUCTION

The increasingly demanding signal and image processing requirements for on-board payloads comes from issues such as the need for more bandwidth, higher sensor resolutions and sensitivities, better data compression, more accurate and adaptive calibration techniques, spacecraft autonomy and more. The current generation of space-qualified DSP's, however, does not meet the requirements of advanced missions anymore. ESA recently initiated the development of a next generation DSP ASIC (1 GFlops), but it will probably take up to a decade before such a component can be brought into production. Therefore, for the shorter timeframe, an alternative must become available. NLR and EONIC currently develop such an alternative: a generic On-board Payload Data Processing (OPDP) module.The OPDP ensures applicability in a broad range of mission applications with a minimum of (re-)development costs. It is reconfigurable, reprogrammable and modular and supports an extensive set of existing and future interfaces such as SpaceWire, SpaceFiber, MIL-1553, CAN, and other high-speed data links, and is therefore compatible with ESA-advocated payload data handling architectures [1].
The OPDP combines the computing power of two ESA-initiated key components: i) the LEON-2-FT general purpose RISC processor [2], developed by Gaisler Research AG, Sweden, and produced in rad-hard technology by Atmel; and ii) the 4 GFlops programmable Fast Fourier Transform Co-processor FFTC [3], developed by EONIC and licensed to ESA, space qualification by Astrium, and to be produced in rad-hard technology by Atmel before end 2010.
The above items have been the baseline for the OPDP requirements, specification, and architectural design studies [4, 5] and resulted in the design as presented in this paper.
The OPDP shall be capable to perform data processing as an independent processor in a payload architecture. This means that the OPDP may receive assignments from a higher level controlling processor after which the operations are executed autonomously.
The OPDP shall be able to perform high-speed data processing for applications where FFT-oriented operations are involved, including

- SAR image formation processing
- Frequency-domain SAR raw data compression
- SAR complex image compression
- Range compression in altimeters
- SAR mode altimetry processing

- FIR filtering
- Spectrometers

Besides the regular processor instructions, the OPDP shall excel in FFT-oriented instructions, all with complex data, such as one- and two-dimensional (inverse)FFT with or without spectrum shift up to 1 million points; fast convolution, spectrum multiplication, multiply and (inverse)FFT, square law detection, multi-looking, complex ALU operations.
Further a number of special macro instructions are desired to perform high-speed data reduction such as: additional data formatting functions, entropy-coding, quantization, forward error correction, averaging.
Existing and future interfaces can/will be supported such as SpaceWire, SpaceFiber, MIL-1553, CAN, and other high-speed data links. Moreover, the module shall be delivered in combination with an effective application Software Development Environment (SDE). The sustained data throughput rate is 100 Msamples/s (64 bits complex numbers). Besides controlling the FFTC co-processor, the LEON2 processor will be able to execute general control and processing tasks in parallel.

2 FFT CO-PROCESSOR ASIC

Available space-qualified DSP based modules offer a typical computing power of 20 MIPS and more noticeably 20 MFLOPS to 60 MFLOPS. Although it was considered sufficiently high a few years ago, future space applications like raw SAR data compression, radar altimeter processing, optical image processing and even on-board SAR image generation, require a much higher computing power while keeping a substantial level of configurability and flexibility. Therefore the “Fast Fourier Transform Co-Processor” (FFTC) was favoured by ESA for space applications,.
The design of the FFTC is based on the commercially available PowerFFT™ processor IP licensed by ESA from Eonic B.V.[3]. The PowerFFT is the world's fastest and most powerful programmable FFT-centric floating-point DSP, able to process 100 million complex samples per second in continuous mode, with a rich set of functionalities for Fast-Fourier Transforms (FFT) computations and FFT-based algorithms, including N-dimensional FFTs, correlations and convolutions. The PowerFFT is a mature ASIC, implemented in numerous military and commercial applications.
The PowerFFT has a 64 bit primary input port, 64 bit primary output port and can execute up to 1K pts FFT or convolution, including windowing, sustained in 10 μs with floating point precision. Four additional I/O ports are available for 4 optional SDRAM (or SRAM) bank extensions for long FFTs, FFT based multi-dimensional algorithms, overlapped algorithms, and (double buffered) corner turning operations.
The flexibility of the memory bank type is guaranteed by using an Address Generator FPGA, which allows cost-effective memory use, easy adoption to addressing schemes, easy upgrades to larger memories, and specialized memory use for space and military applications. A standard instruction set for the PowerFFT is available for FFT macro-functions (≤ 1M pts. 1D FFT / convolution / correlation, ≤ 1K × 1K pts. 2D FFT / convolution / correlation). Upgrade instruction sets can be developed for large (> 1M pts.) 1D, (>1K × 1K pts.) 2D and multi-dimensional FFT-based algorithms (user specific), and other FFT-like Fast Transforms such as Chirped-Z Transform (CZT).
The PowerFFT supports the following standard data formats:

- 32 bit IEEE floating point (parallel or sequential I&Q);
- 32 or 16 bit integer (parallel or sequential I&Q);

And the following specialized data formats:

- 16 or 32 bit sign inverted integer (parallel and sequential I&Q);
- 2×24+9 bits hybrid floating point;
- 2×12+8 bits hybrid floating point.

The PowerFFT runs on a 100 MHz I/O clock maximum, and a 128 MHz internal processing clock.
ESA plans to make this device available to European industry as an ASSP (Application Specific Standard Product).

3 MODULE ARCHITECTURE

Fig. 1 and 2 show the hardware and the software architectures of the OPDP module, respectively.
The OPDP includes three key components: the LEON2 Fault Tolerant processor ASIC (AT697), the FFTC and the RTAX2000S FPGA. Besides the own data and program memories of the LEON2, in addition six 2 Gbit SDRAMs are accommodated on the board. Four of them are directly connected to the FFTC for efficient and high-speed processing operations. The two other SDRAMs serve as data buffers for input and output streams. The various data paths can be interconnected using a 64-bits wide Switch Fabric offering maximal flexibility. The board includes a broad range of interfaces: up to three SpaceWire connections for data I/O, and optionally two high-speed serial links for which SpaceFiber is an attractive candidate. A fourth SpaceWire connection, and /or a CAN-bus or a MIL-1553 bus can be used as command & control interface.

Inside the FPGA the various interfaces and functional blocks are interconnected by a System-on-Chip AMBA bus, offering internal modularity. The LEON2 processor is able to program the FFTC and the Switch Fabric by blocks of macro-sequences which can be downloaded into a firmware-based control sequence processor, after which the data processing of a block or a stream can be executed at maximum speed. In the meantime the LEON2 is able to perform other tasks.
Optionally, the two SDRAM data buffers can be connected to the LEON2 memory bus, as shared memory. This allows high-speed data transfer between LEON2 and the SDRAMs, because the PCI-bus is limited to about 30 Mcycles/s. For some applications, such as SAR processing, this option doubles the performance of the board. For example a SAR scene consisting of 4000 rangelines of 5000 complex samples can be completely processed into a detected image within 11 seconds [5].
A so-called User Block is included to perform user-defined operations on a data stream, which would otherwise take too much LEON2 processor time and which cannot be performed by the FFTC. One example is entropy coding for data compression. The LEON2 processor controls the FFTC, the Switch Fabric and the various interfaces via the PCI bus.
All the SDRAMs are protected by EDAC functionality against bit flips due to radiation. The complete module can be implemented on an extended double size Eurocard.
A sophisticated software development environment is required to fully exploit the capabilities of the OPDP hardware. Not only to perform the traditional software development tasks like compiling and linking but especially to generate the aforementioned macro sequences for the FFTC and the surrounding functional hardware blocks. The SDE will also include a simulation of the OPDP hardware in order to validate FFTC command sequences before they are loaded into the actual hardware. The SDE will be based on an open platform and it can be easily extended with tools for a specific application domain (like for instance image viewers for SAR data processing).
The Basic Software (BSW) of the OPDP board consists of a real-time Operating System (RTOS), software drivers to support the hardware interfaces, supporting mission specific software components, like data protocol layers, health monitoring, TM/TC interfaces, and an Application Programmer Interface (API) to command the FFTC and the Switch Fabric. The API is simple and straightforward and it basically refers to command sequences with are prepared in the SDE. For instance a 2D FFT of a 4K by 4K matrix consists of a large number of FFTC instructions but the application invokes this operation through a single call.

4 CONCLUSIONS

There is a clear trend towards more applications using on-board payload data processing and compression.
In this paper an On-board Payload Data Processing module architecture has been presented which can be used in a broad range of mission applications. It is a reconfigurable and reprogrammable module, based on the LEON2-FT, a space-qualified general purpose RISC processor, and the FFTC, a space-qualified FFT-oriented DSP co-processor. The OPDP supports an extensive set of existing and future interfaces such as SpaceWire, SpaceFiber, MIL-1553, CAN, and other high-speed data links, and is compatible with ESA-advocated payload data handling architectures.

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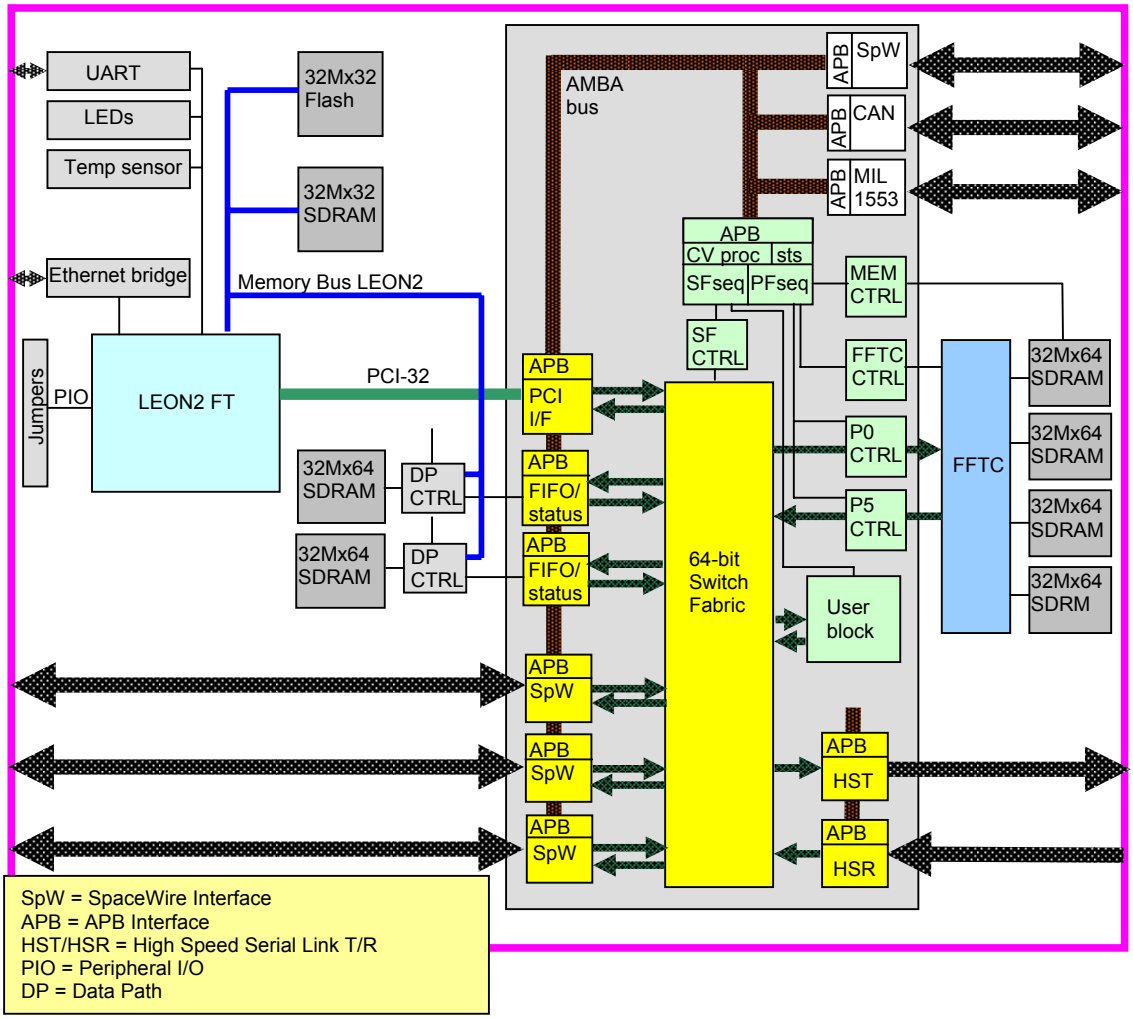

Fig. 1 Architectural block diagram of the OPDP

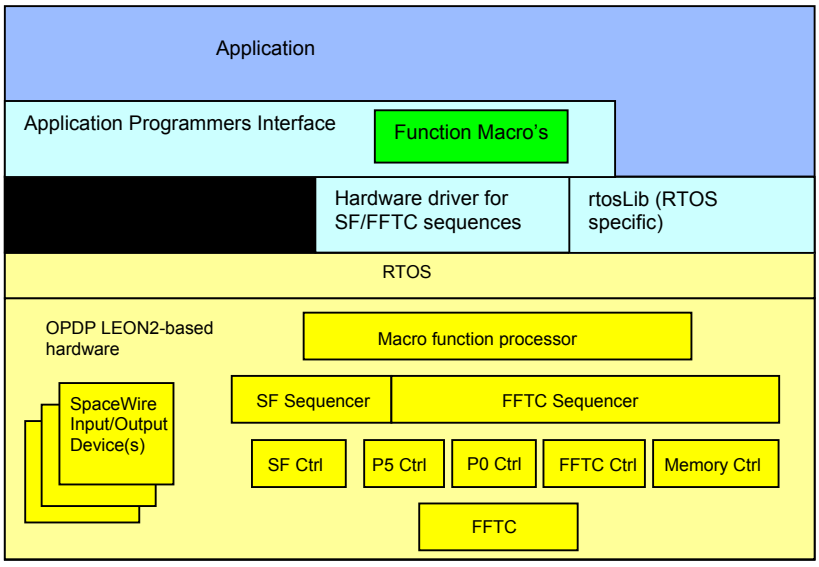

Fig. 2 Software architecture of the OPDP